

FIG. 4

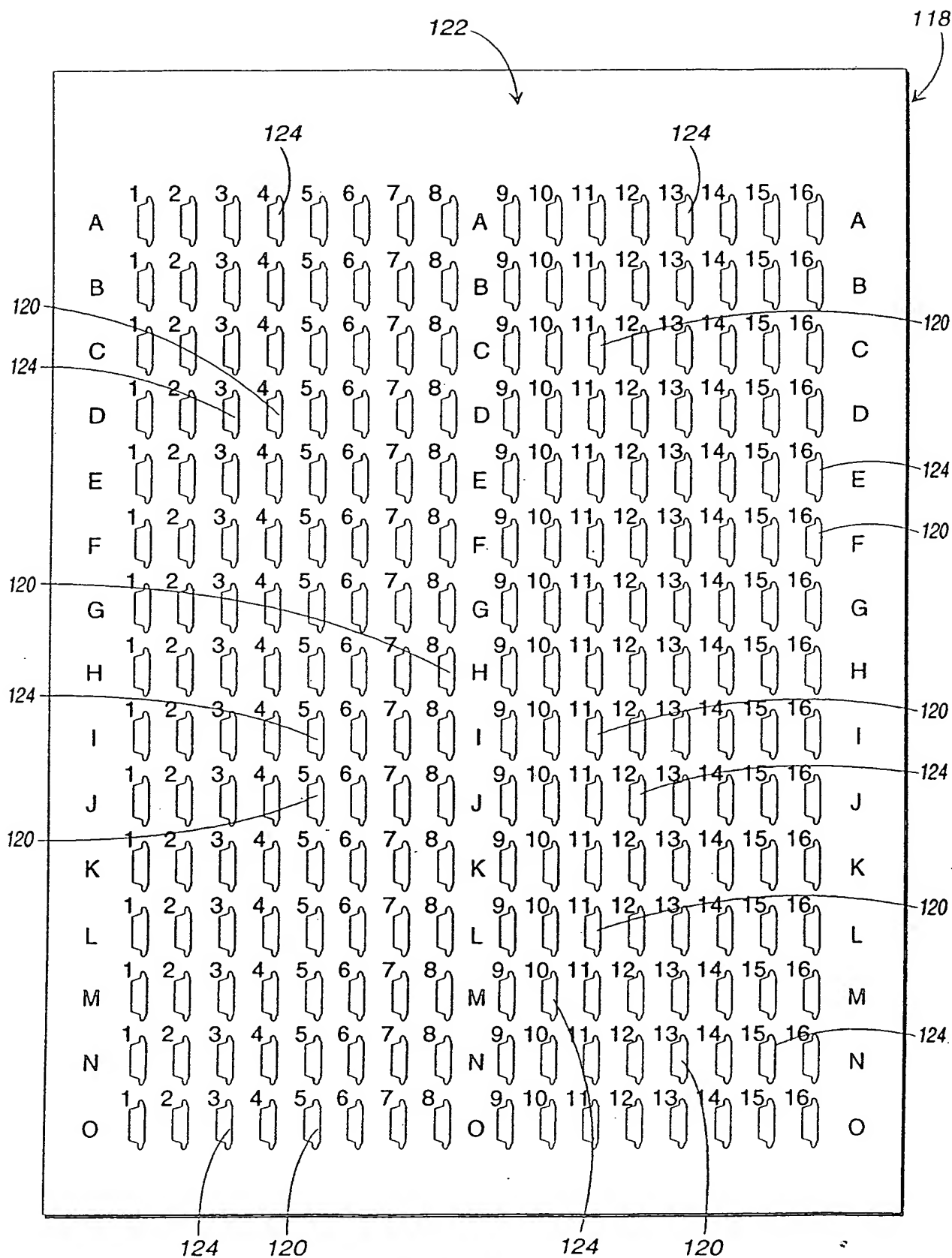


FIG. 5

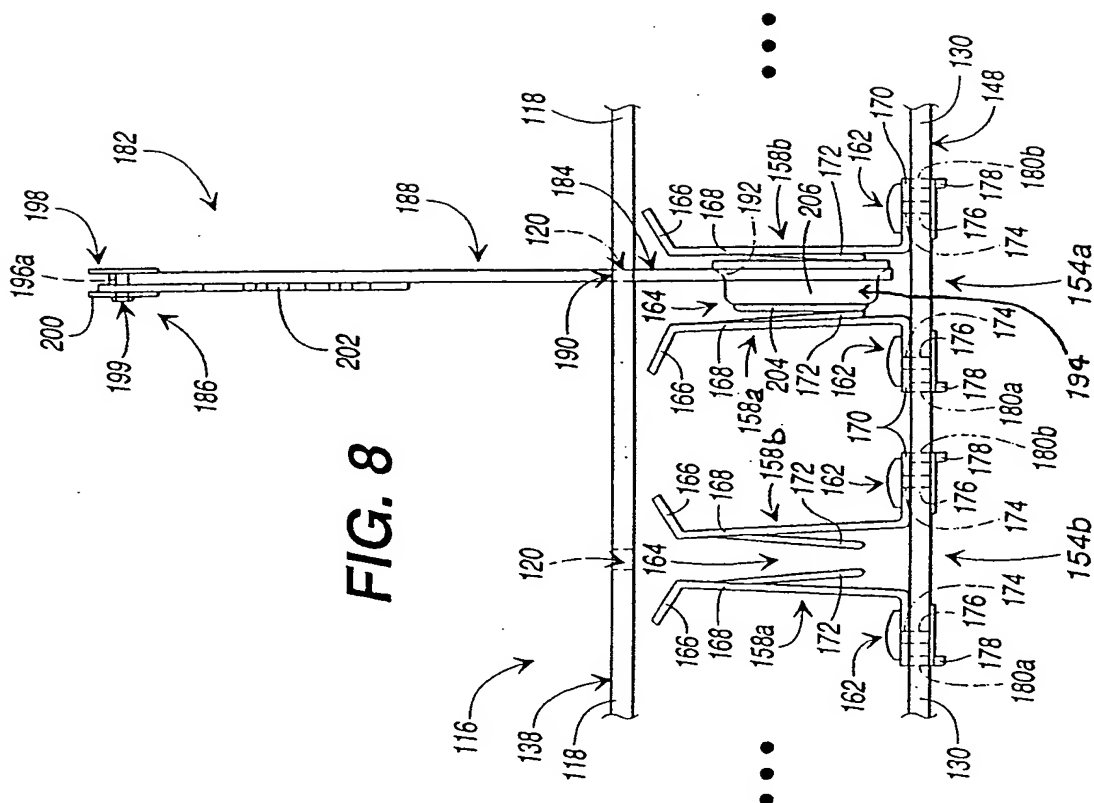


FIG. 7

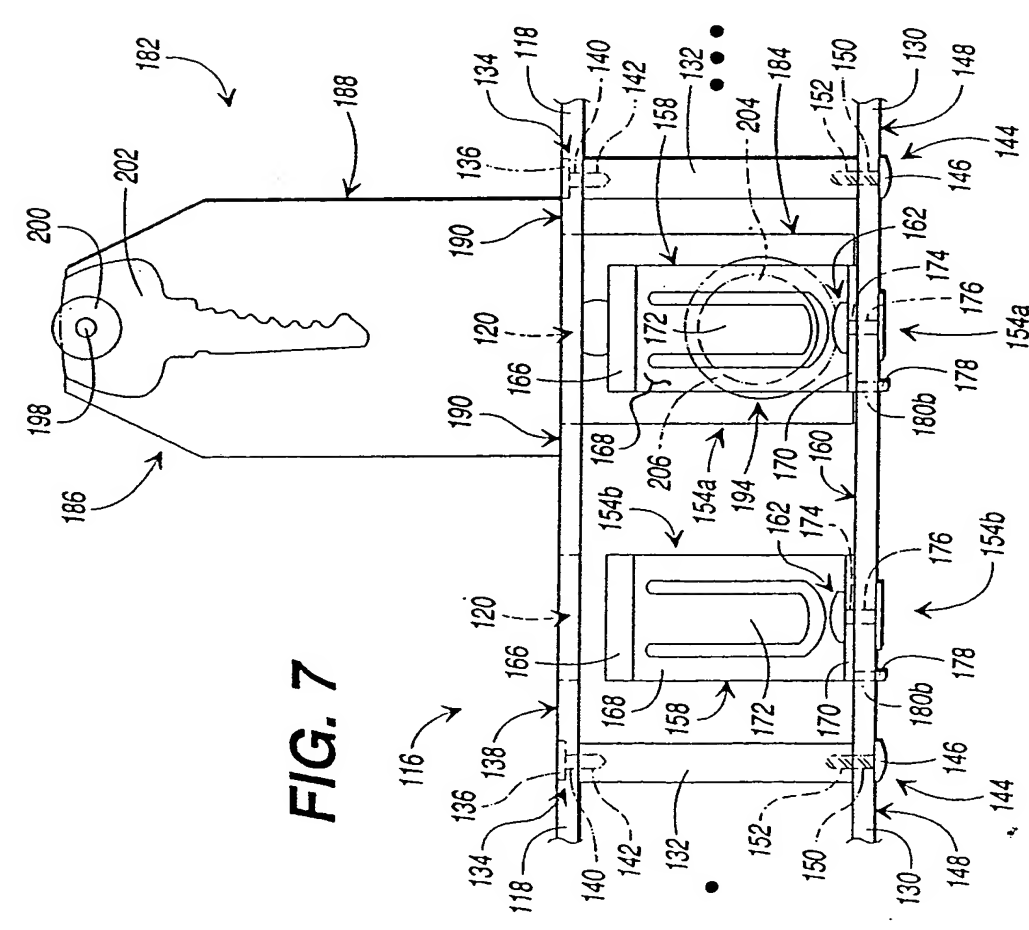
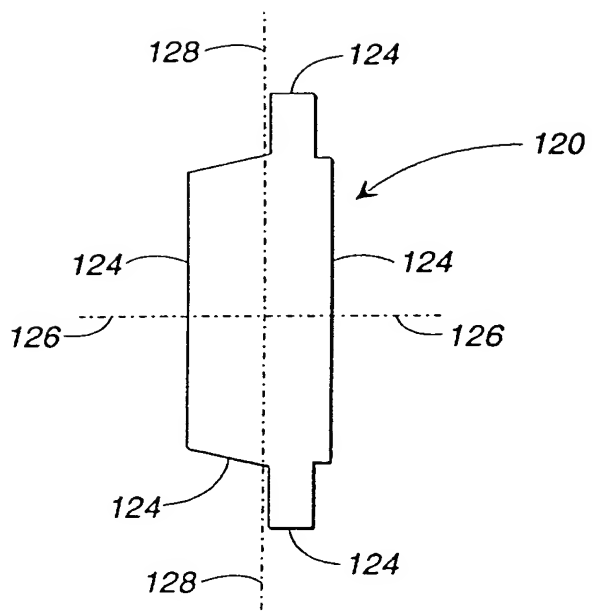
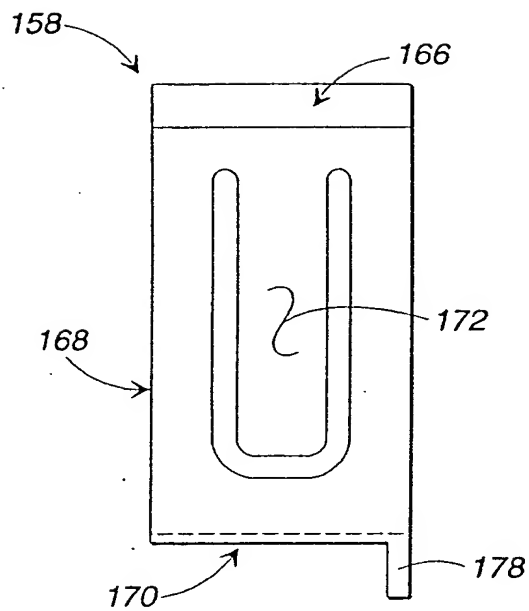


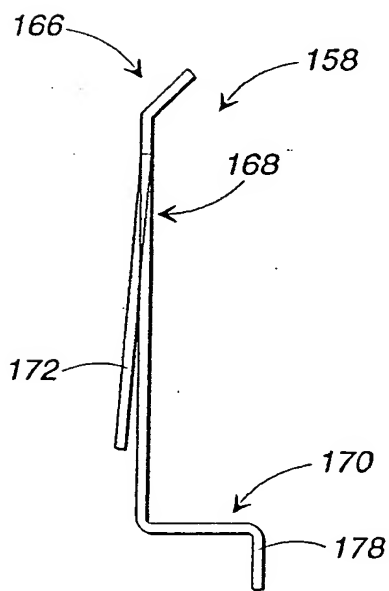
FIG. 8



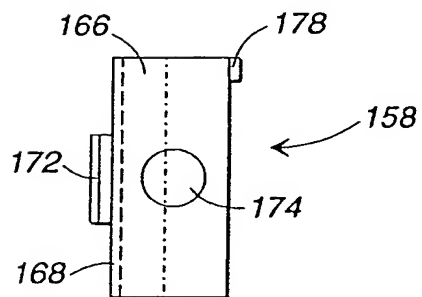
**FIG. 6**



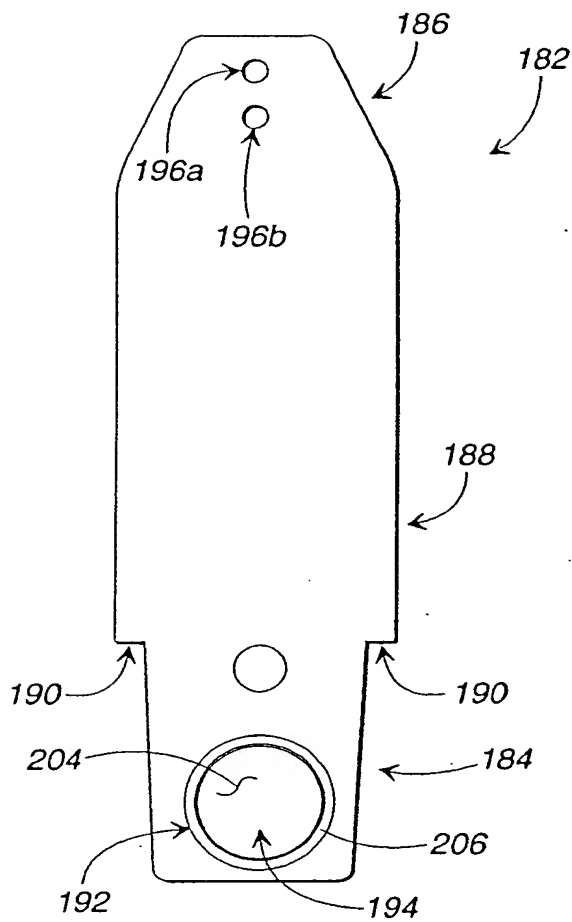
**FIG. 9**



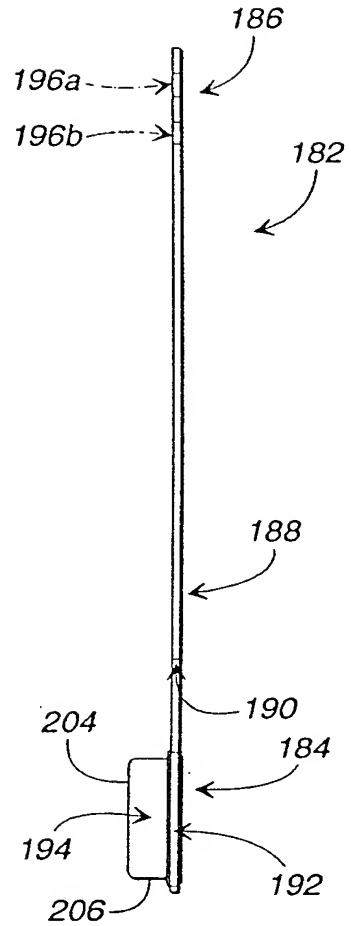
**FIG. 10**



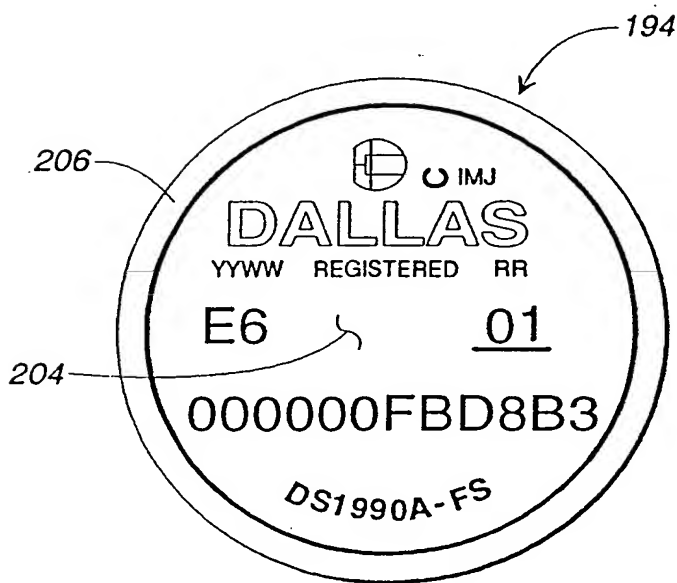
**FIG. 11**



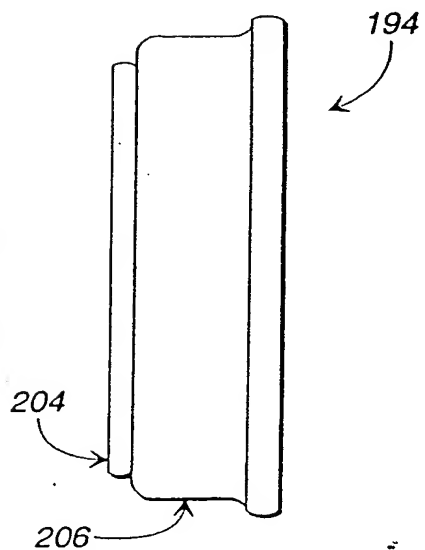
**FIG. 12**



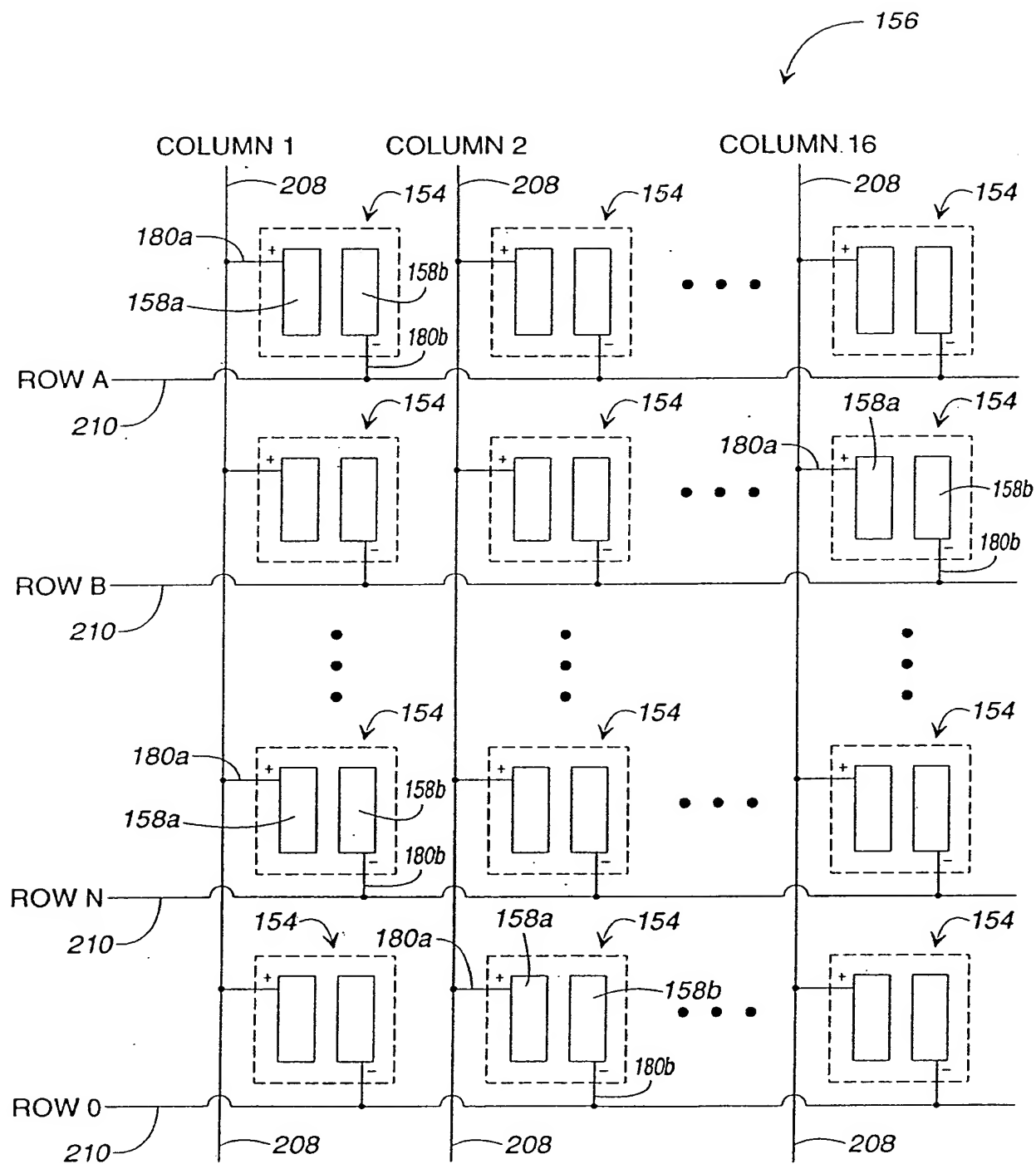
**FIG. 13**



**FIG. 14**

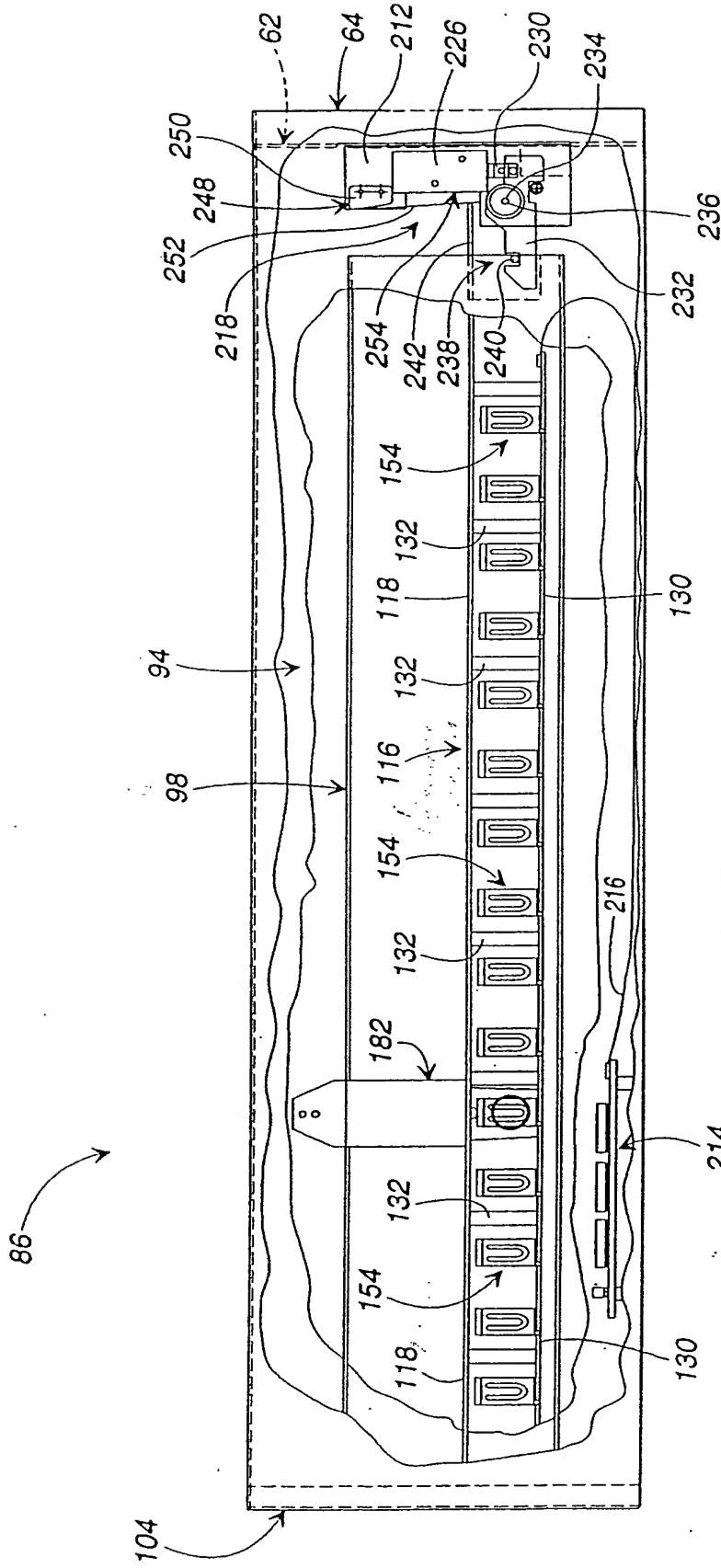


**FIG. 15**



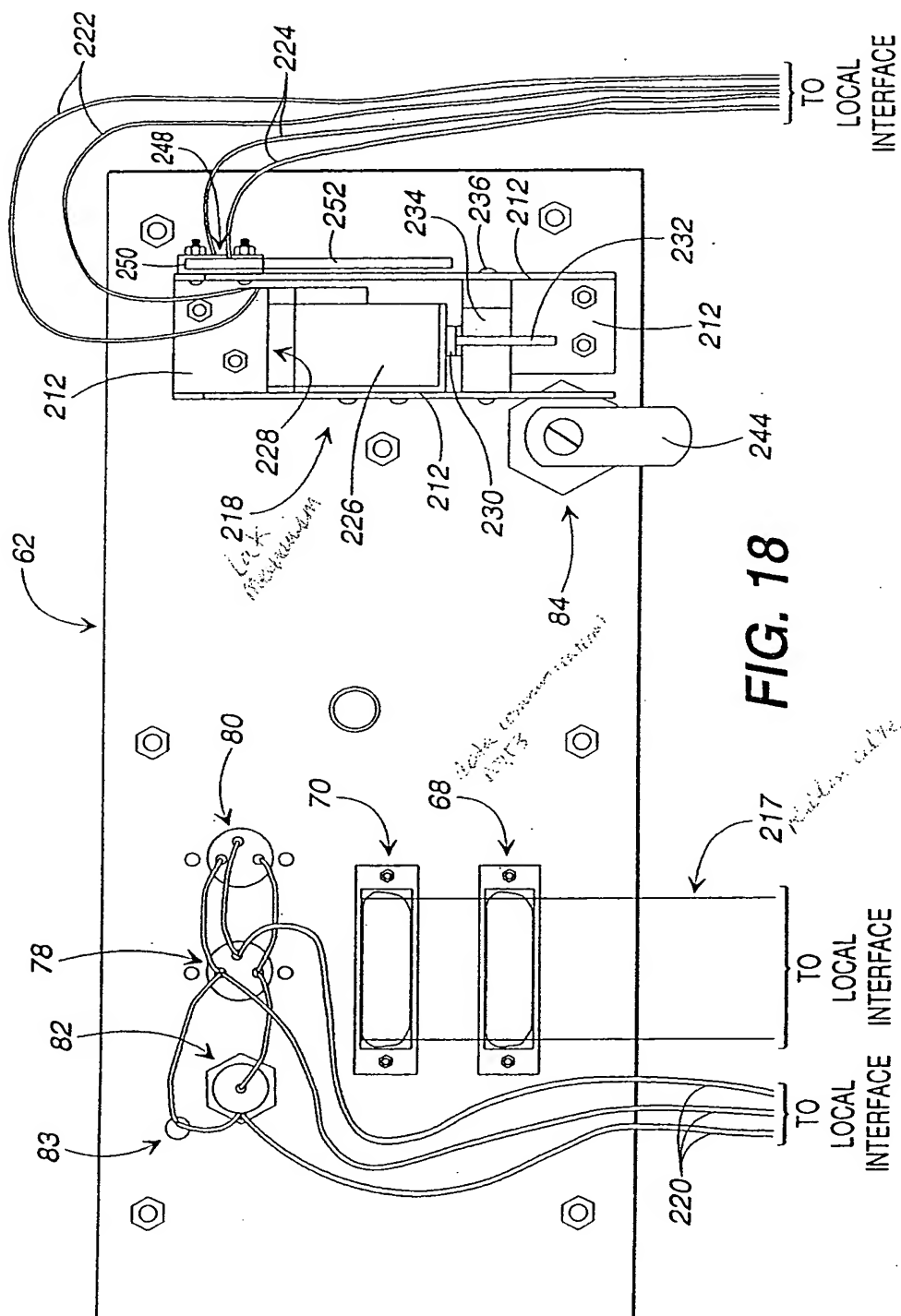
**FIG. 16**





**FIG. 17**

Cable  
 Connects electrical  
 signals between  
 the two  
 processors and  
 backplane.  
 "1016" wire  
 draws in  
 information  
 instead of  
 sending it  
 out.



**FIG. 19A**

The diagram illustrates a power management circuit, labeled FIG. 19A. It is divided into two main functional blocks: 316 (ENABLE DW) and 318 (POWER SUPPLY). Block 316 contains an AND gate with two inputs, one of which is connected to a bus system. The output of the AND gate is connected to a resistor, which in turn is connected to the gate of a MOSFET. A capacitor is connected between the drain and source of this MOSFET. Block 318 contains a diode, a capacitor, and a MOSFET. The diode is connected to a bus system, and its cathode is connected to the gate of a MOSFET. A capacitor is connected between the drain and source of this MOSFET. The circuit is connected to a bus system and a memory array.

MATCH LINE TO FIG. 19C

**FIG. 19A**

316-

318-

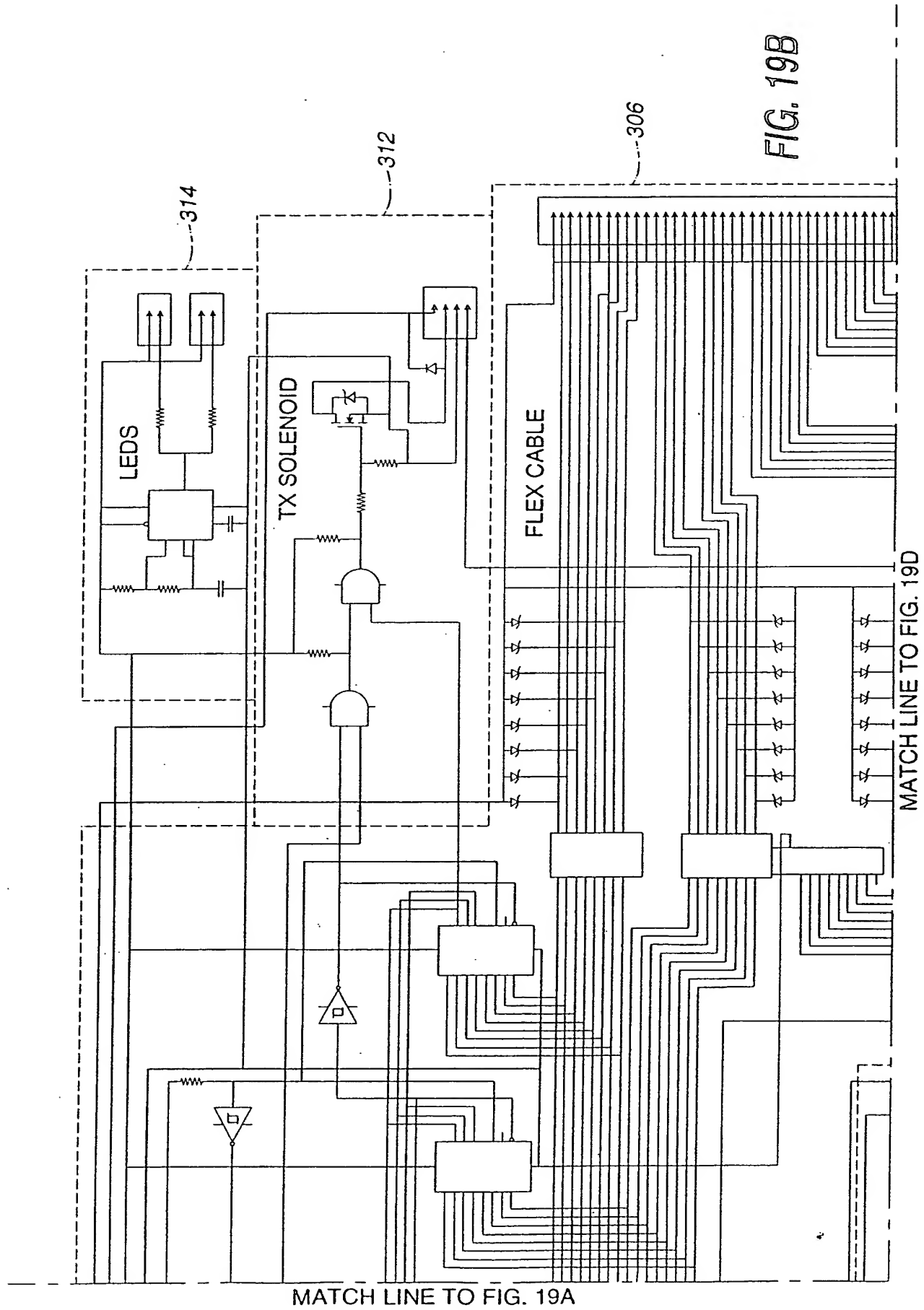


FIG. 19B

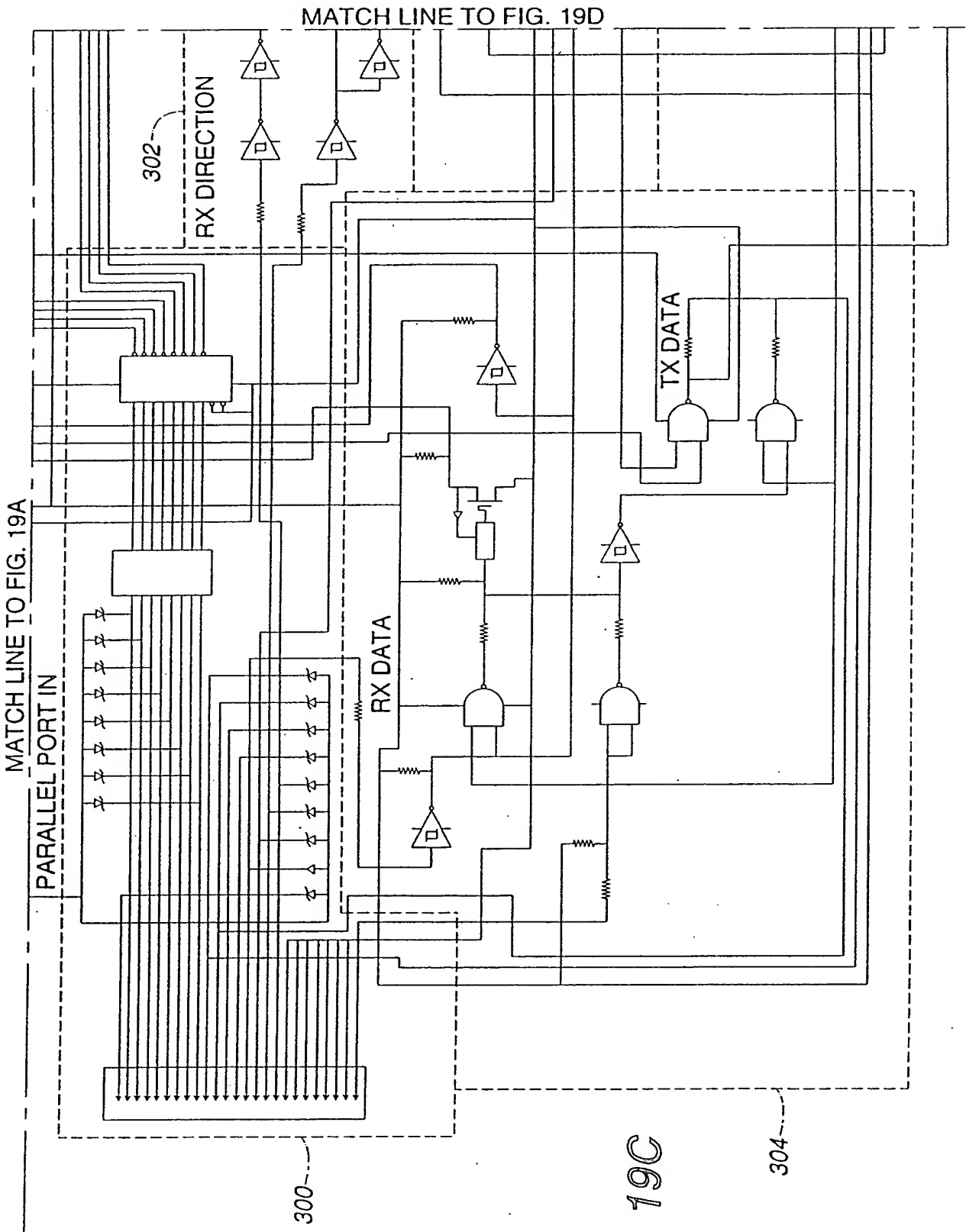
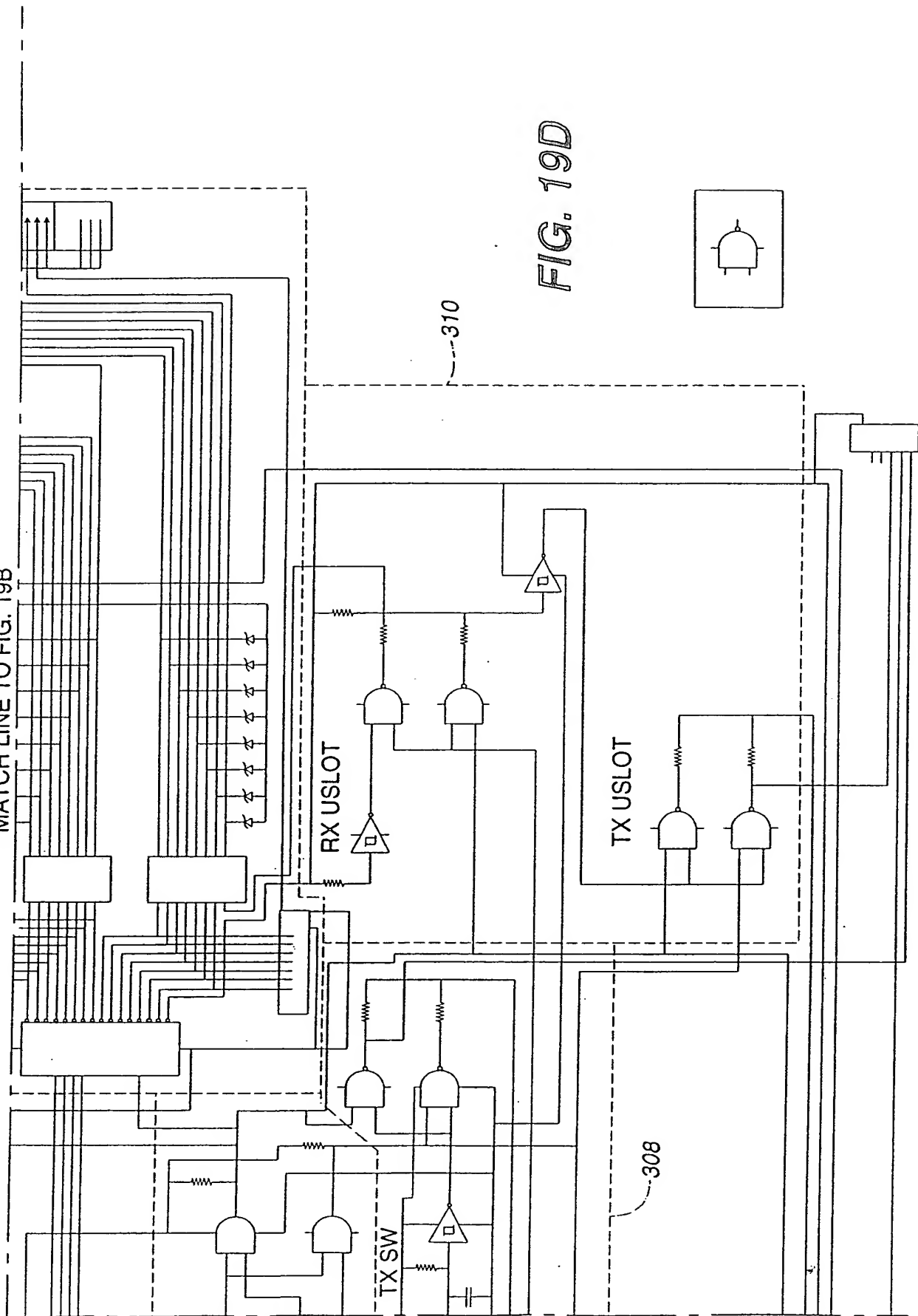


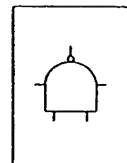
FIG. 19C

MATCH LINE TO FIG. 19B



MATCH LINE TO FIG. 19C

FIG. 19D



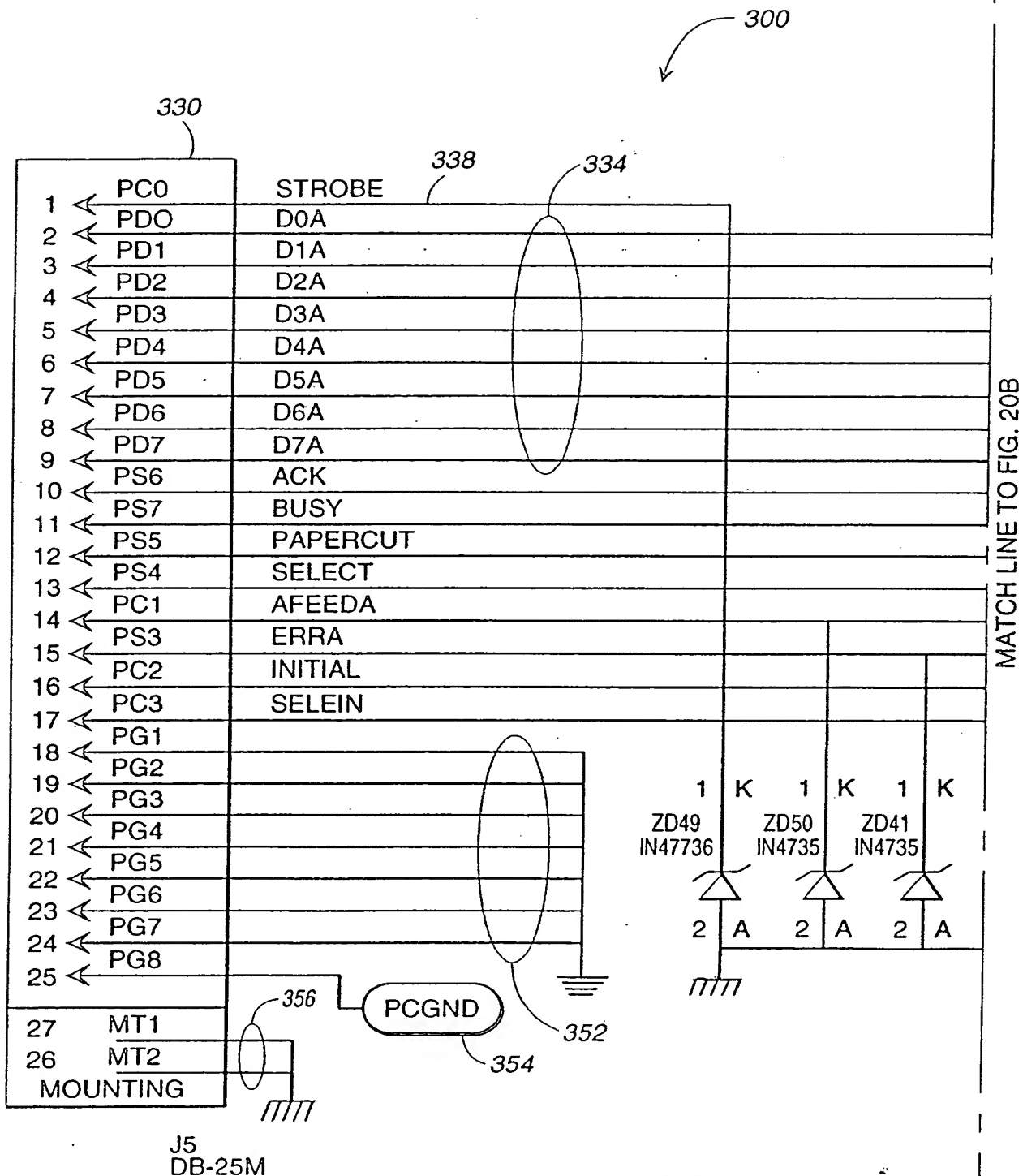
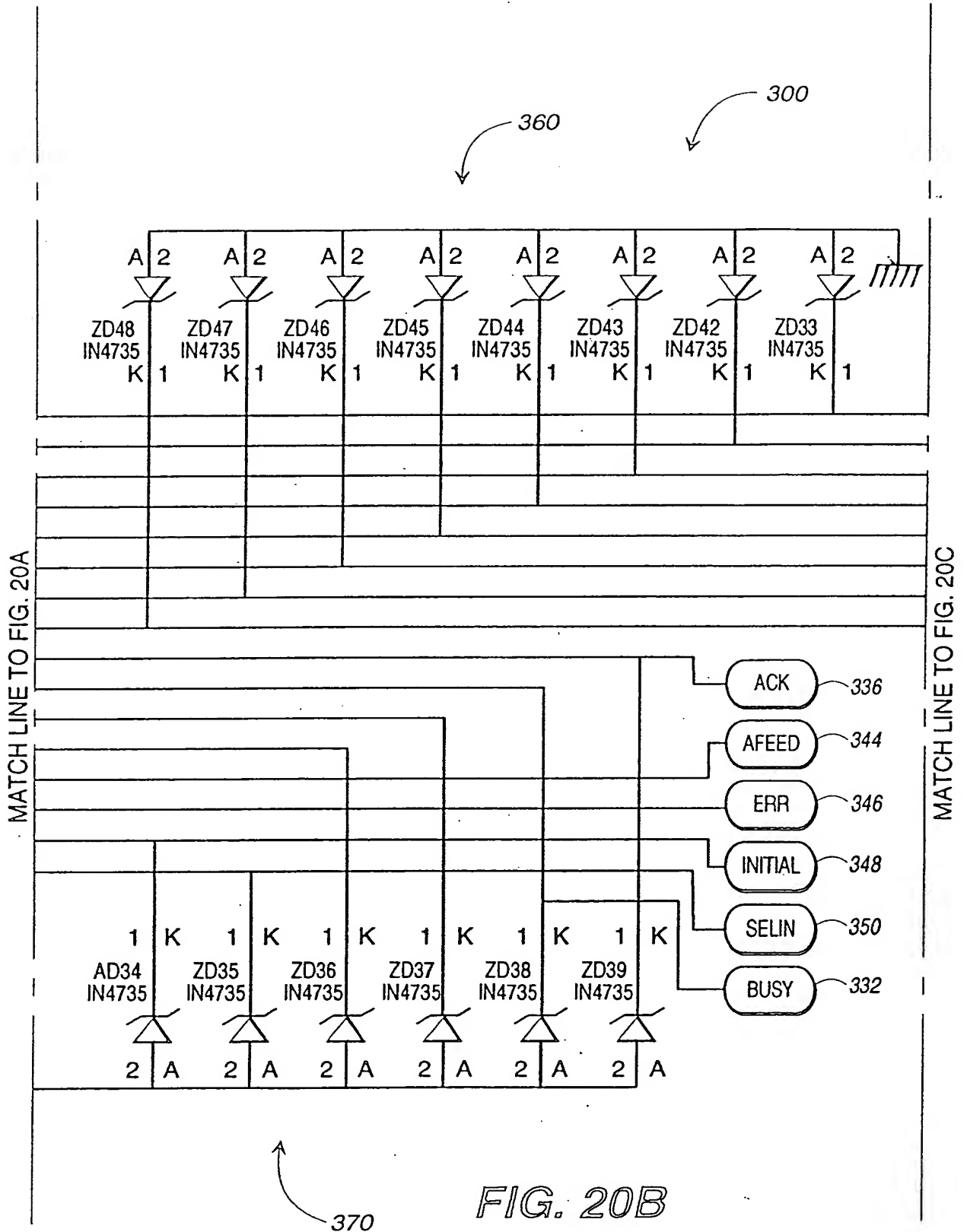


FIG. 20A





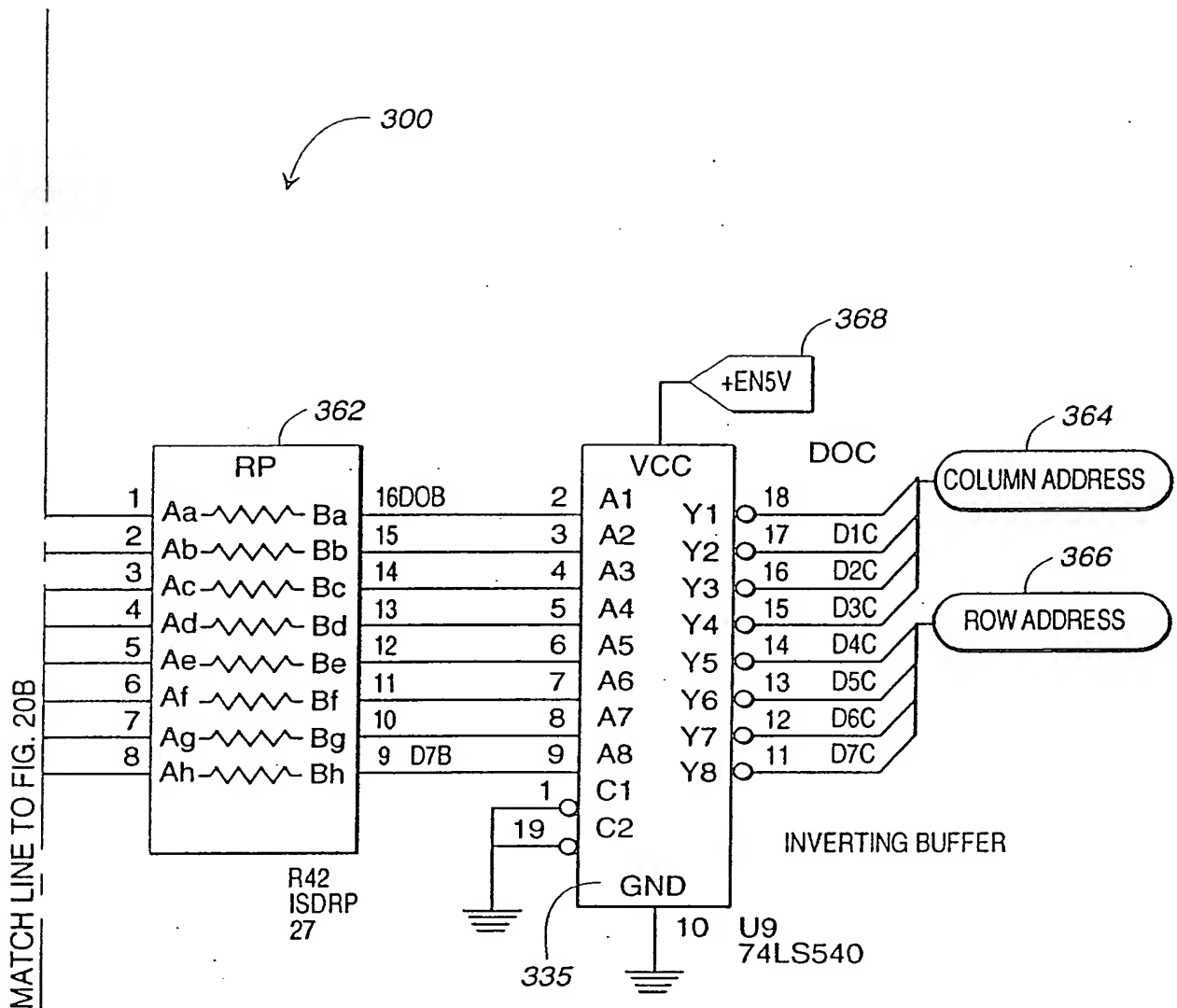
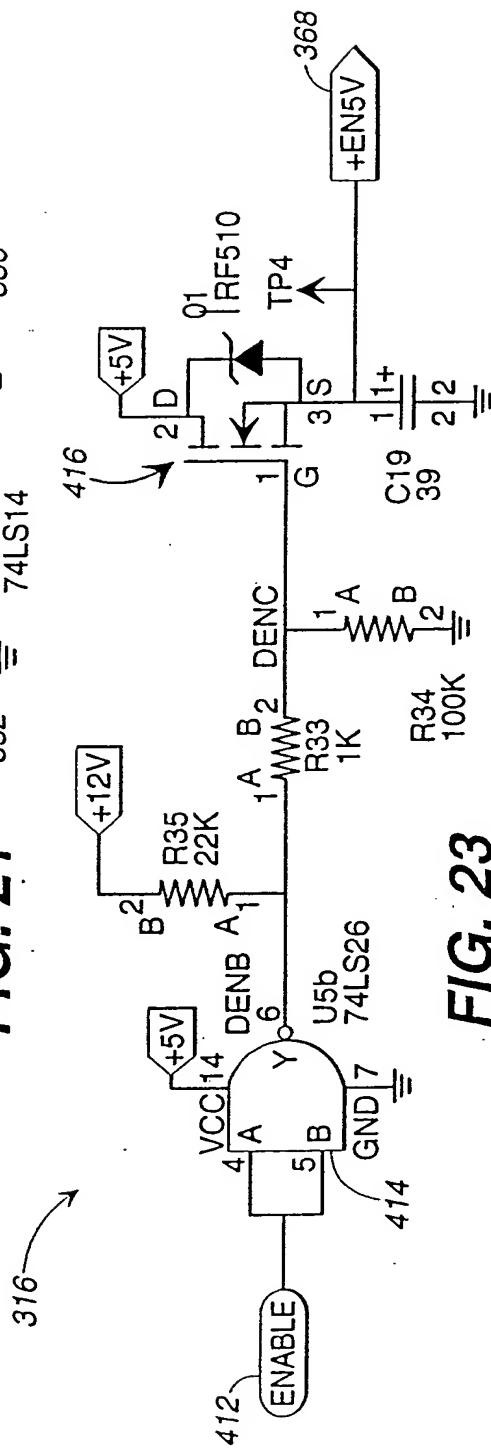
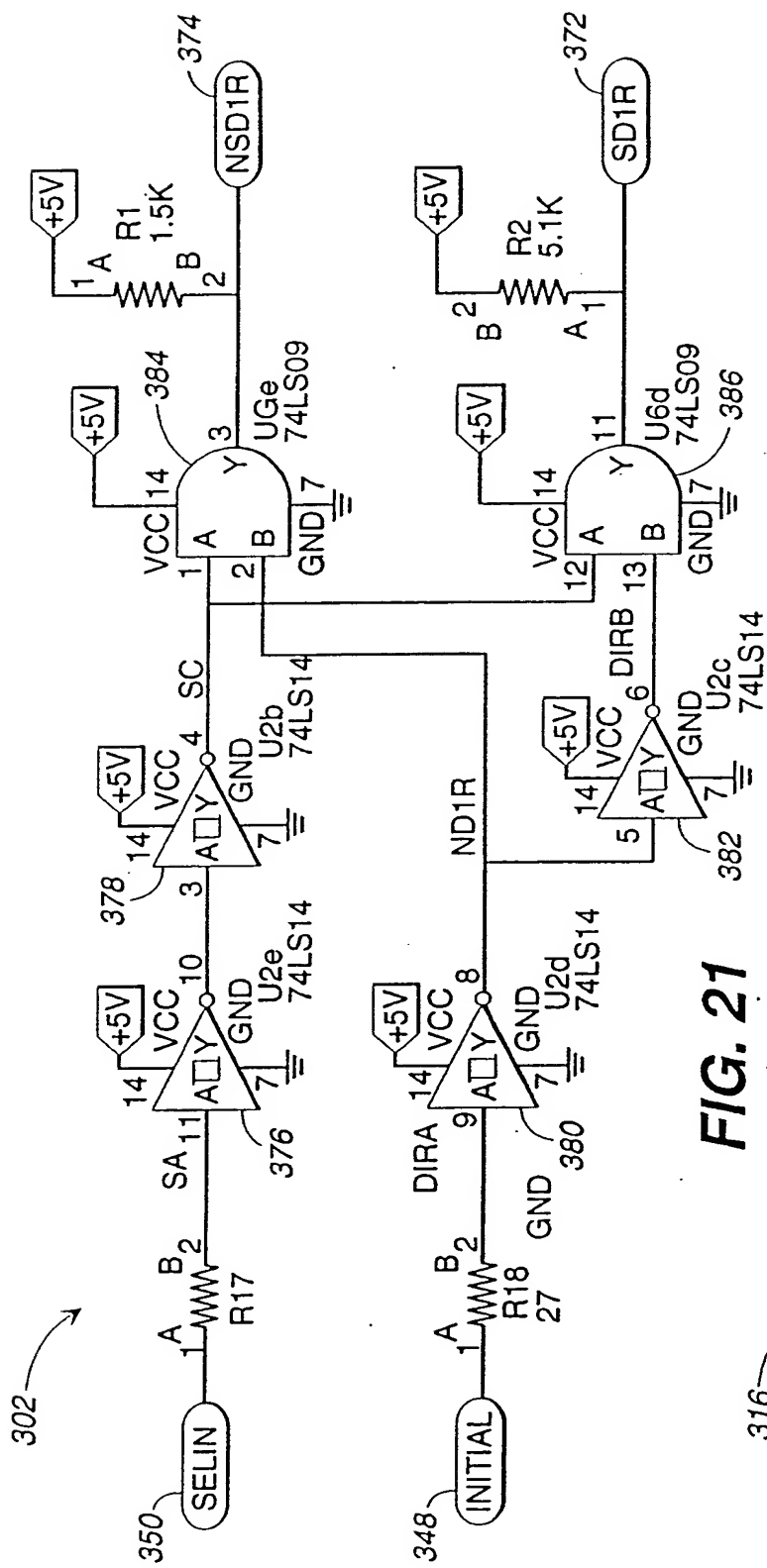


FIG. 20C





MATCH LINE TO FIG. 22A

304

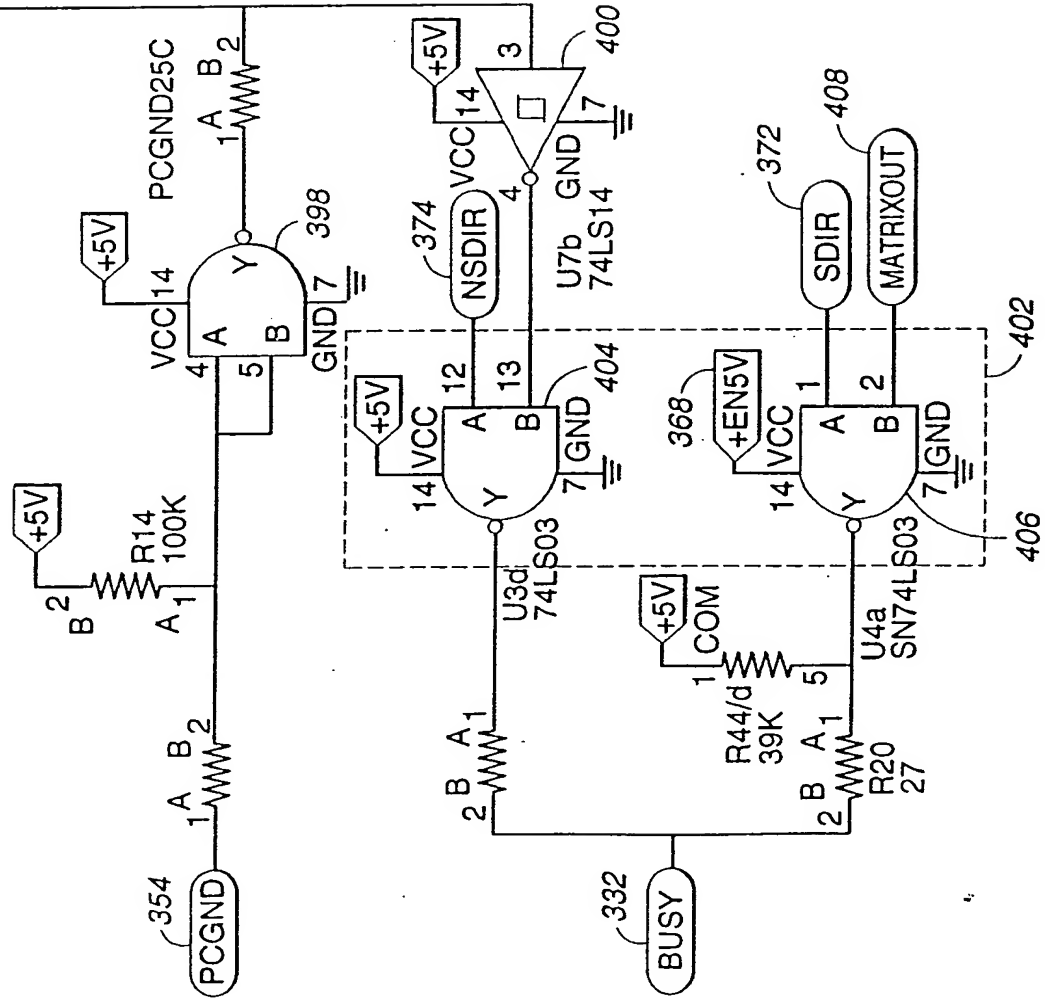
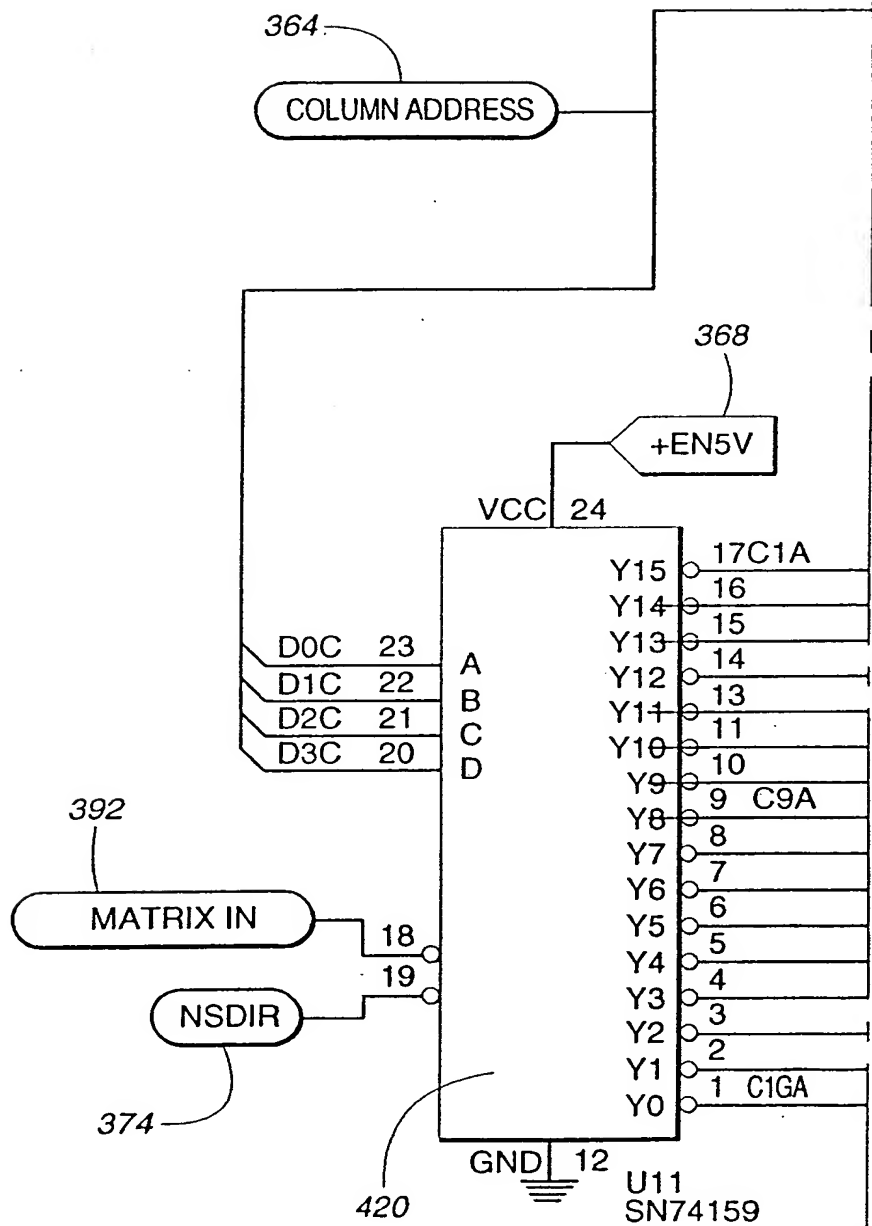


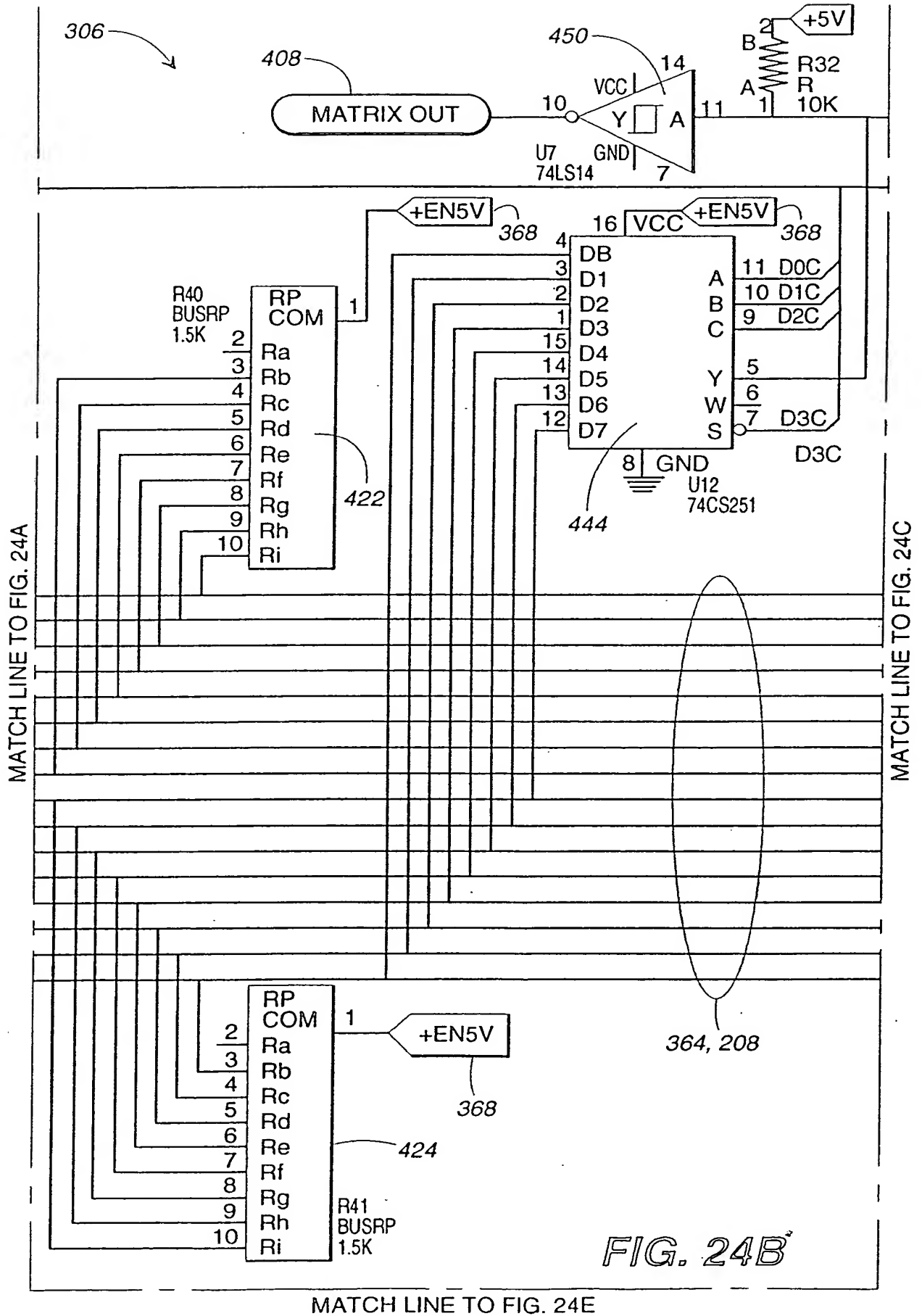
FIG. 22B

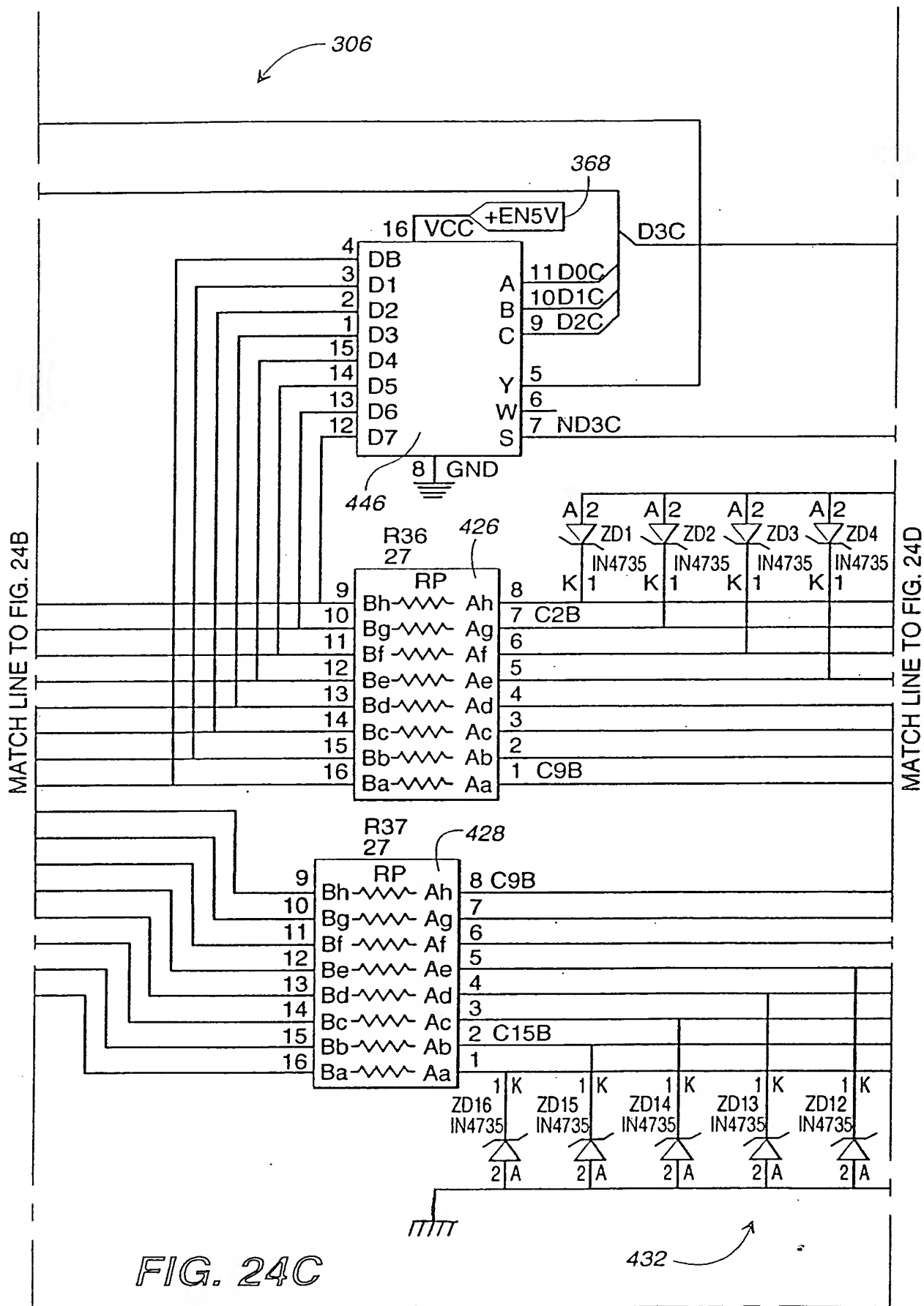
306



MATCH LINE TO FIG. 24B

**FIG. 24A**





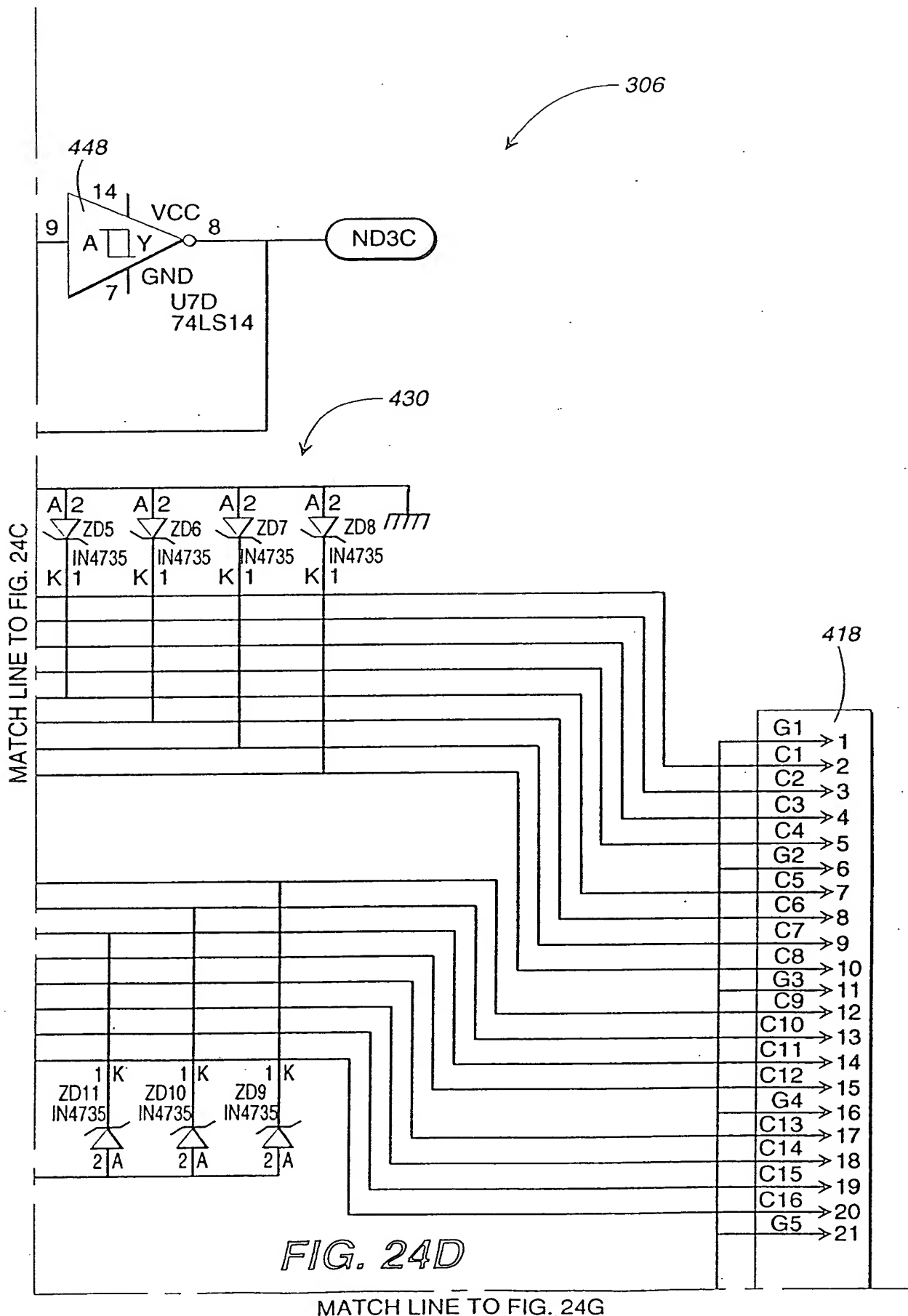




FIG. 24E

MATCH LINE TO FIG. 24C

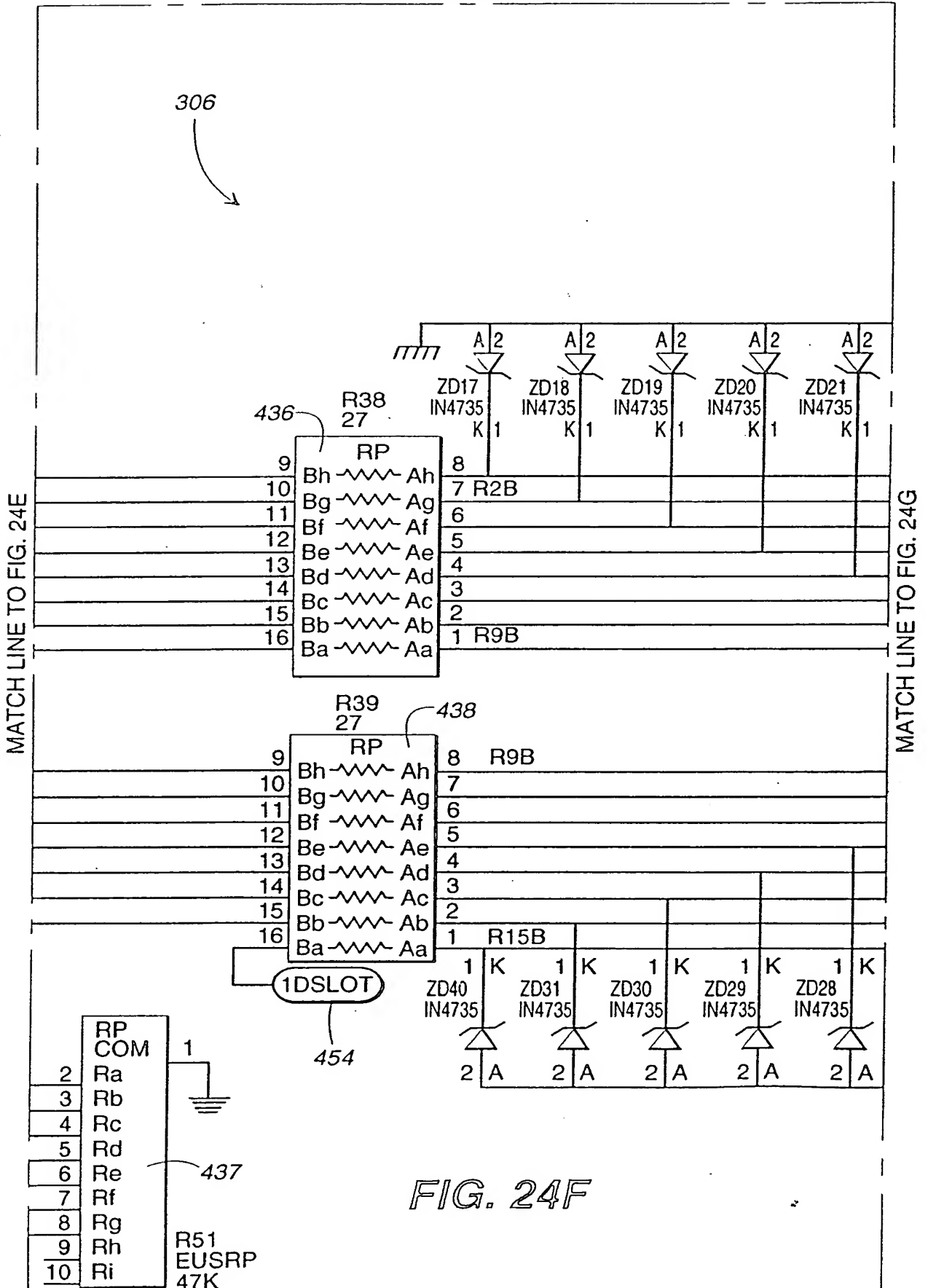
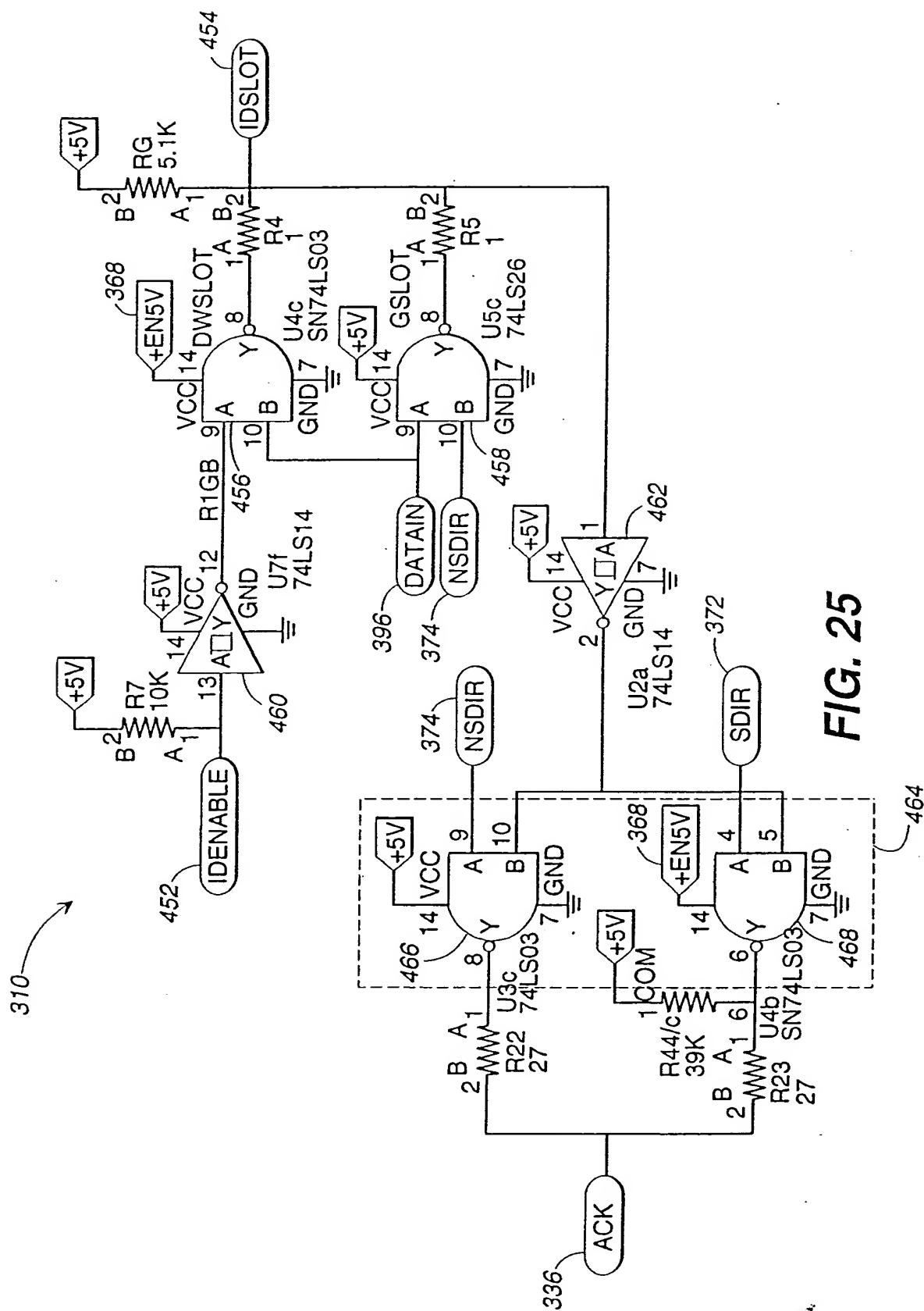
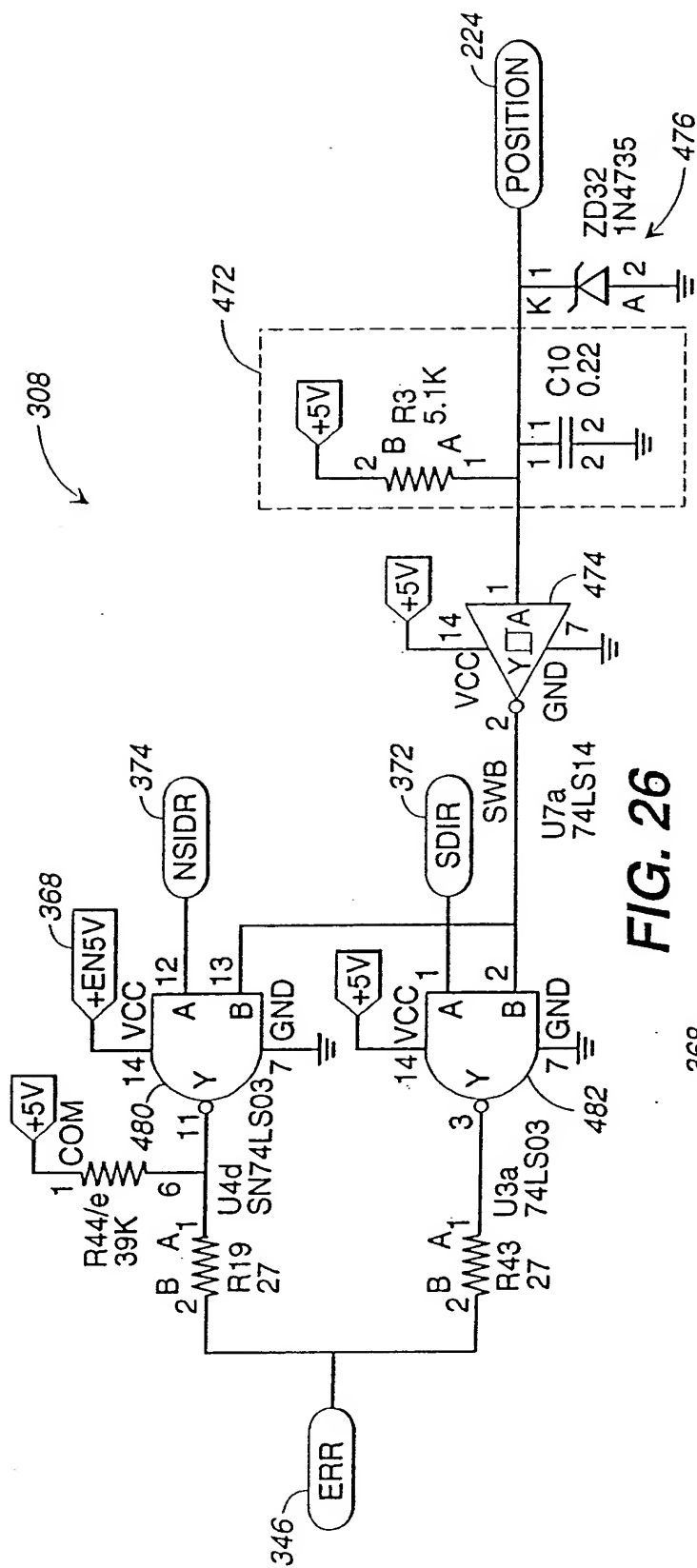


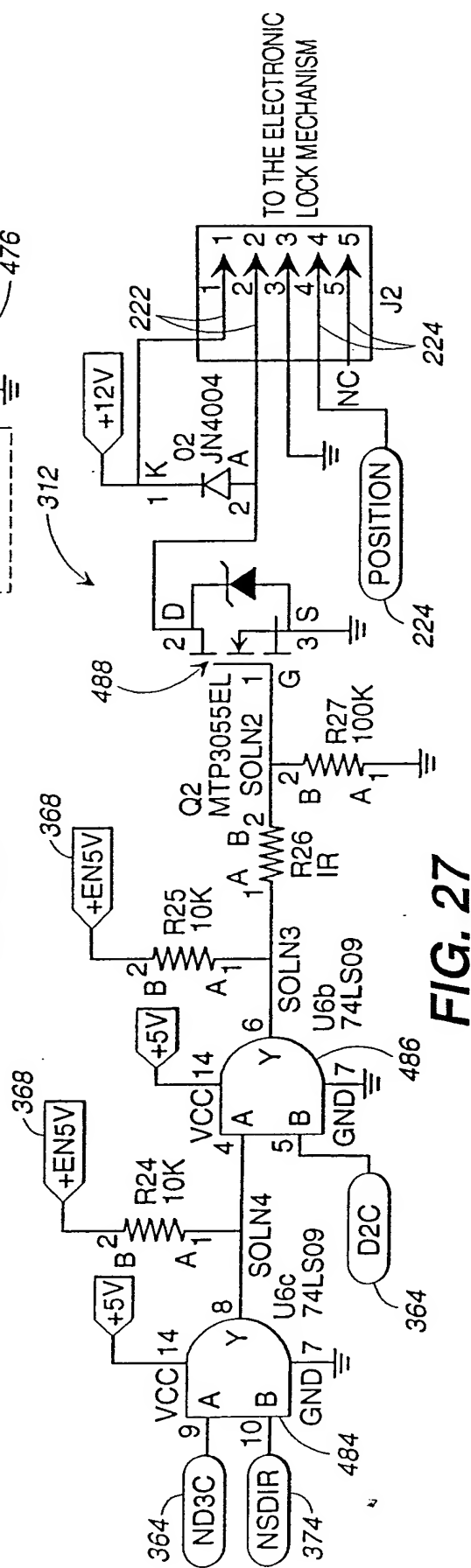
FIG. 24G

FIG. 24G





**FIG. 26**



**FIG. 27**

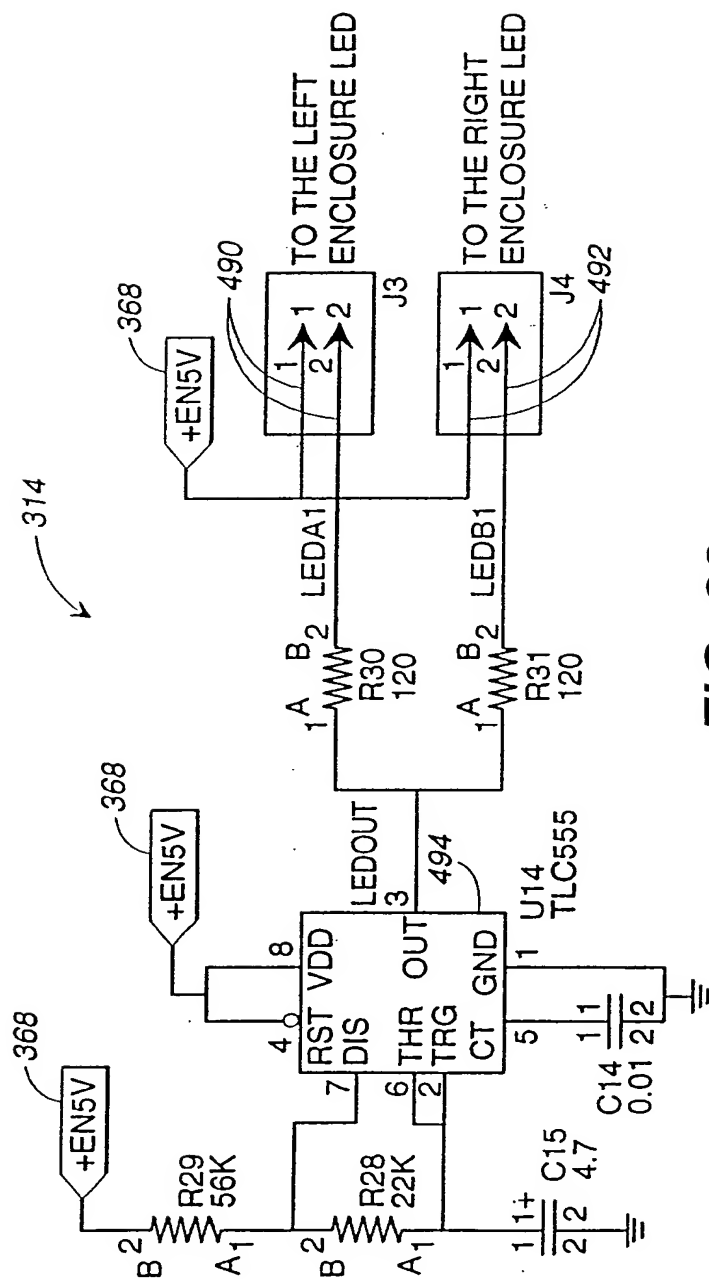
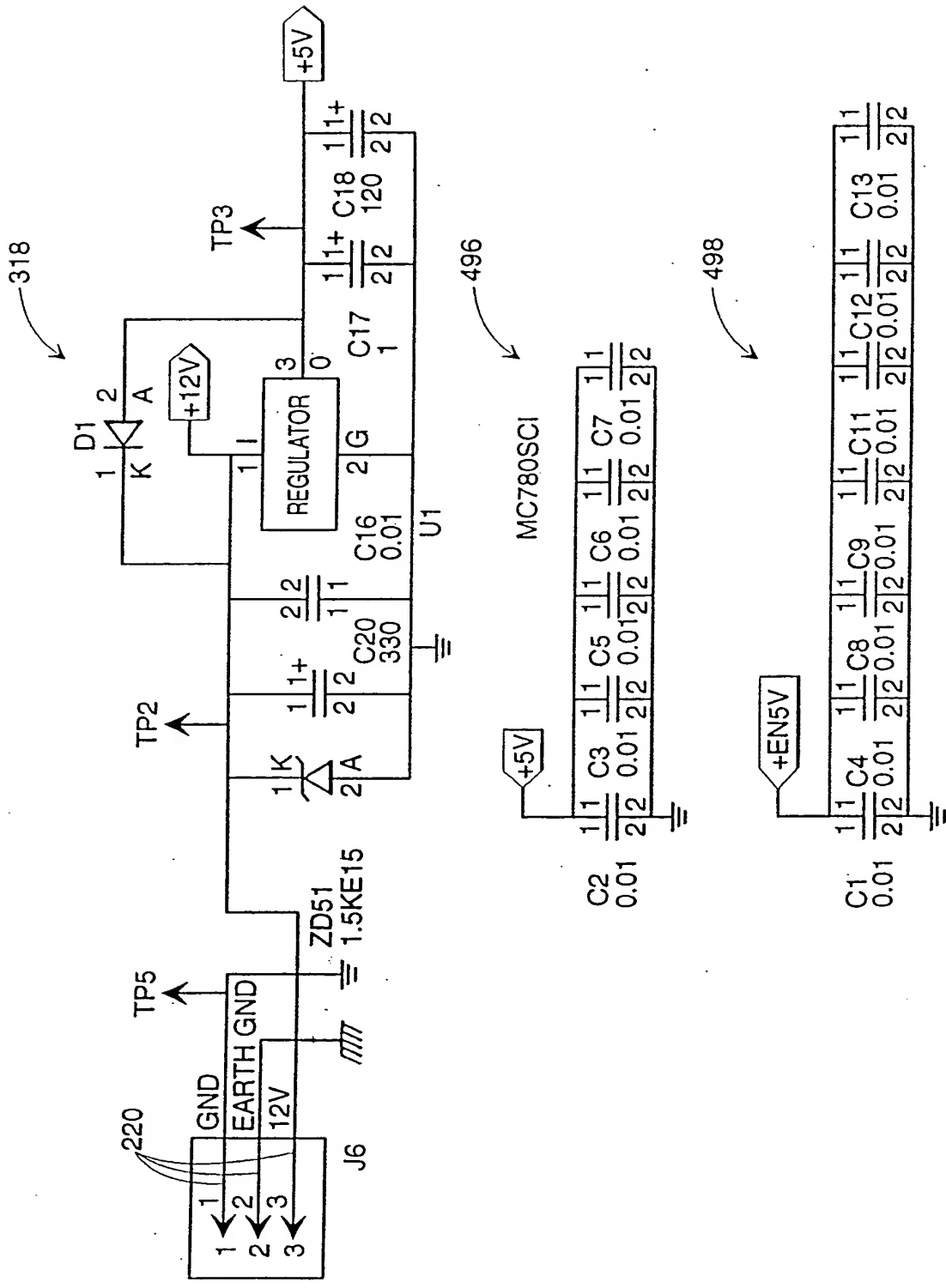


FIG. 28



**FIG. 29**

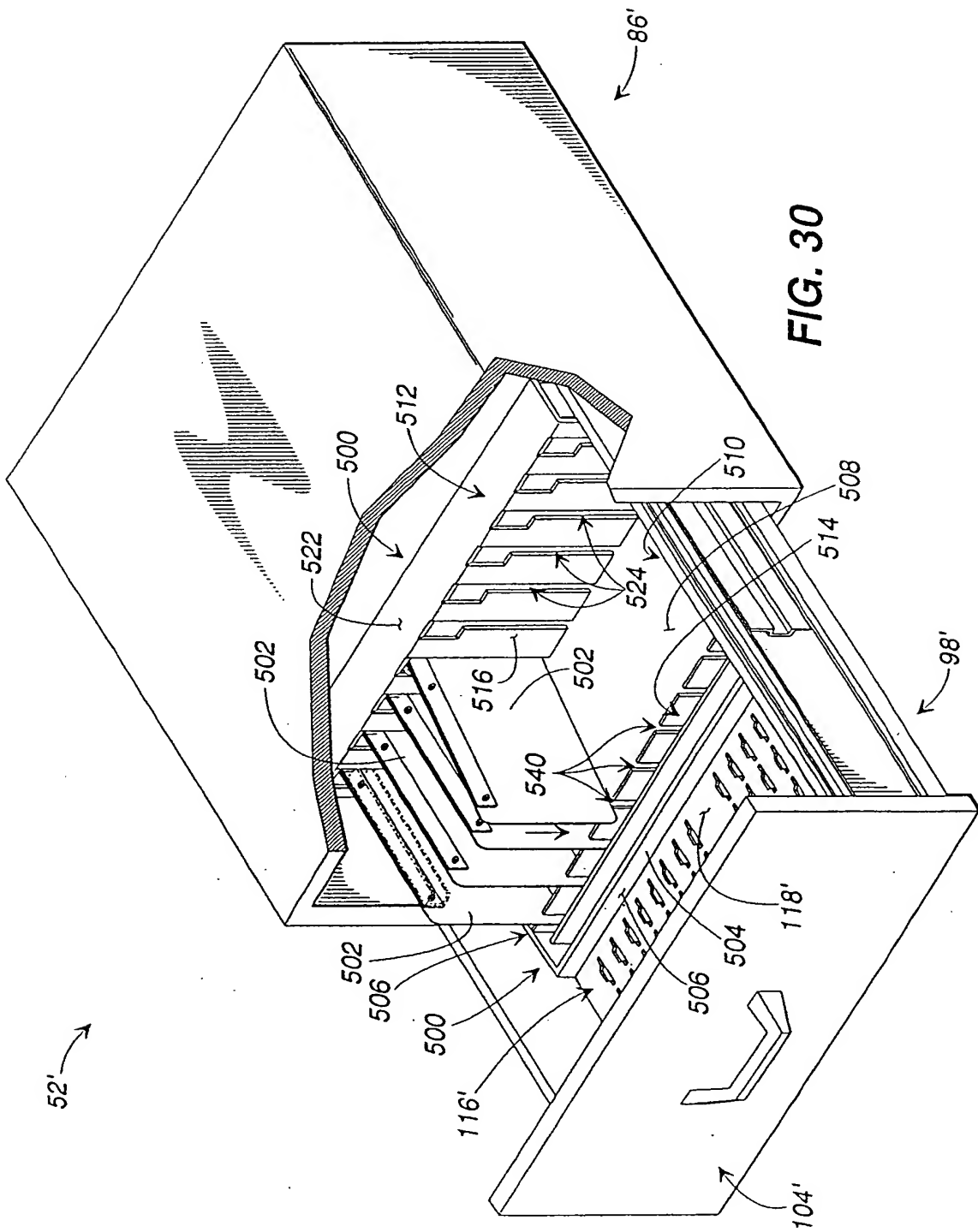


FIG. 30





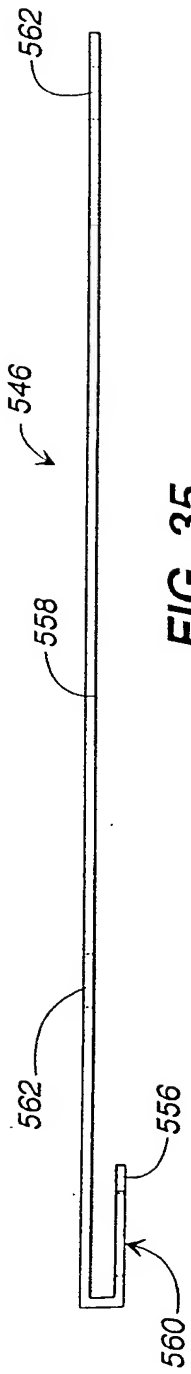


FIG. 35

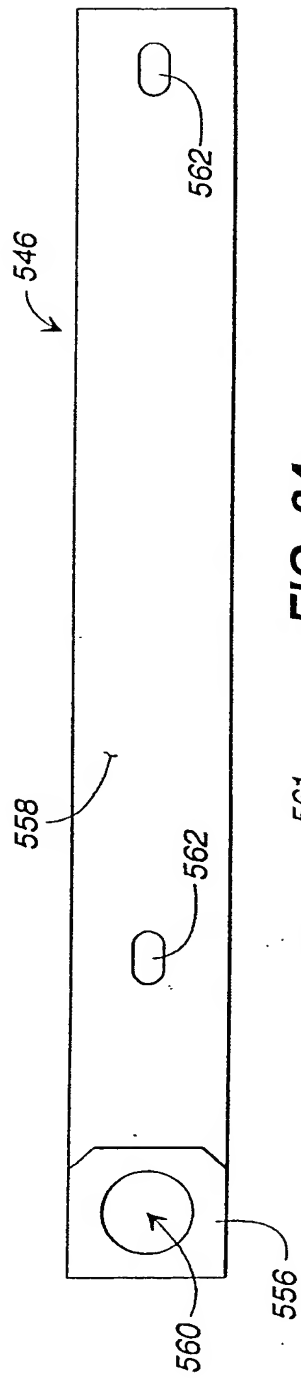


FIG. 34

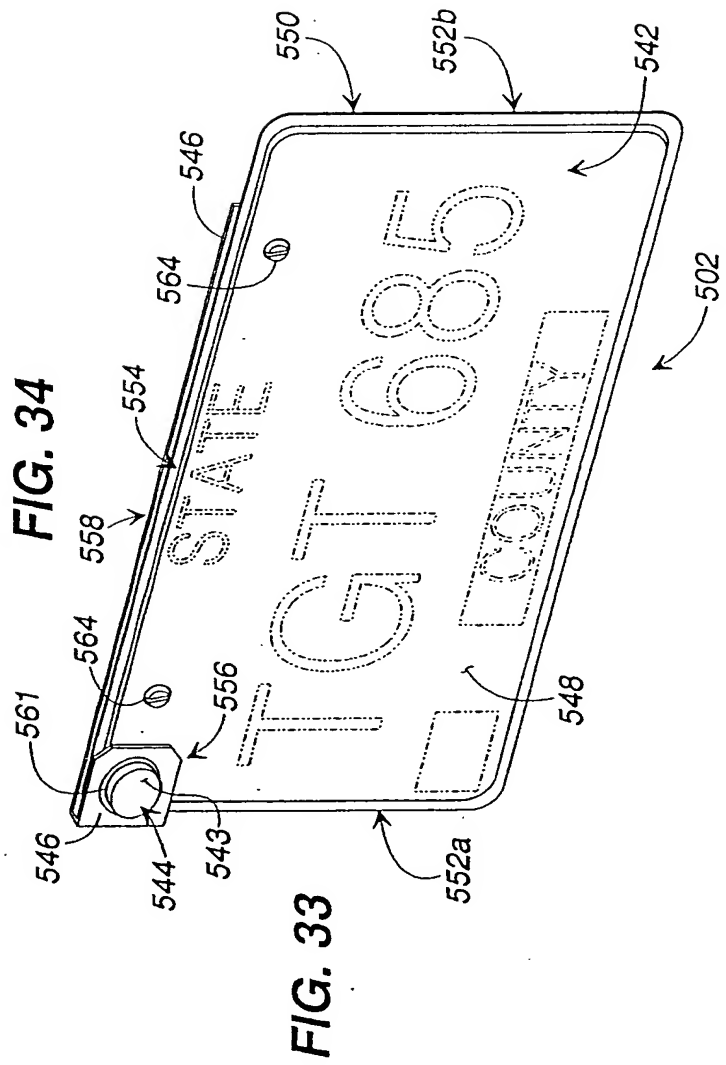
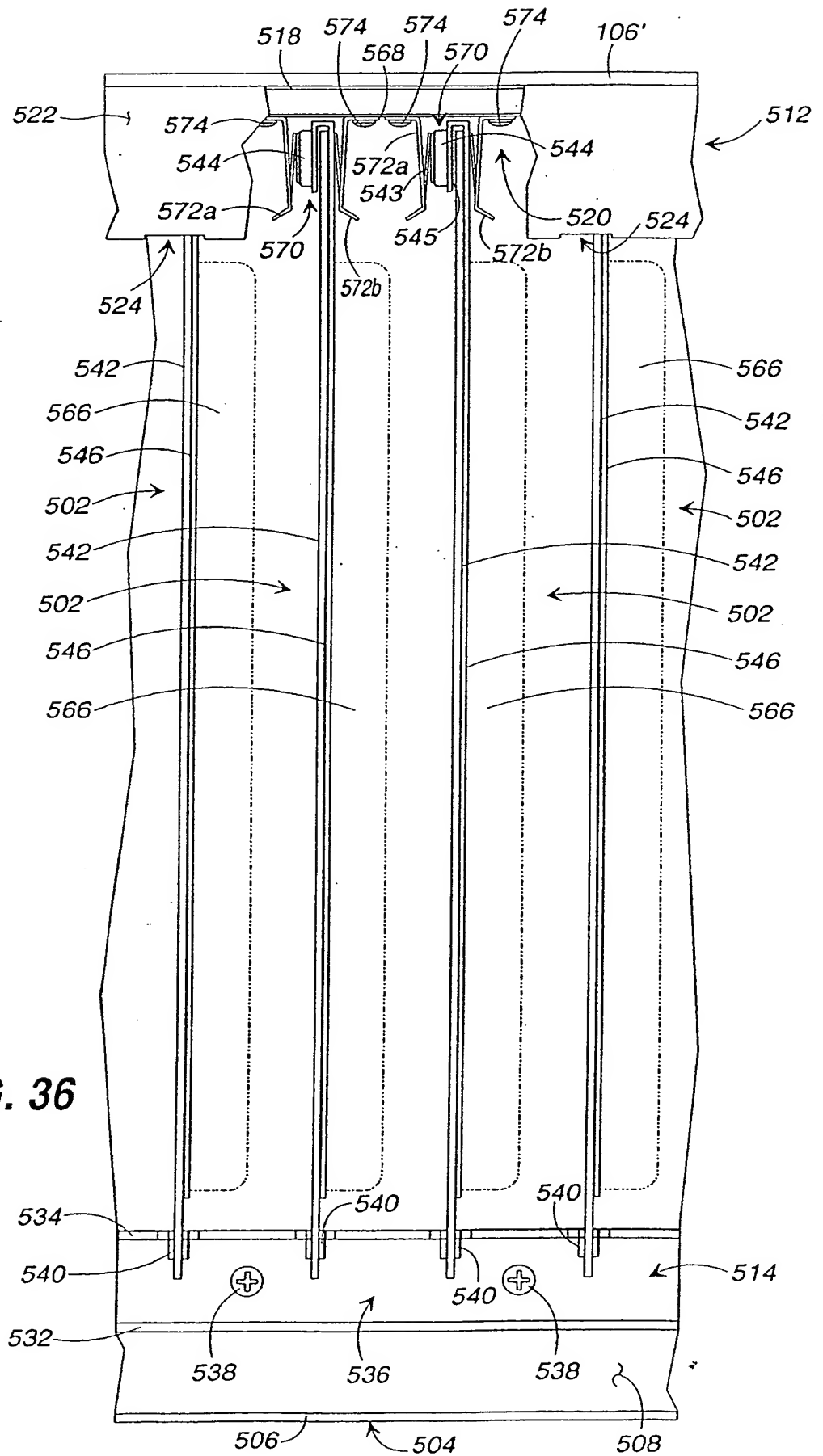
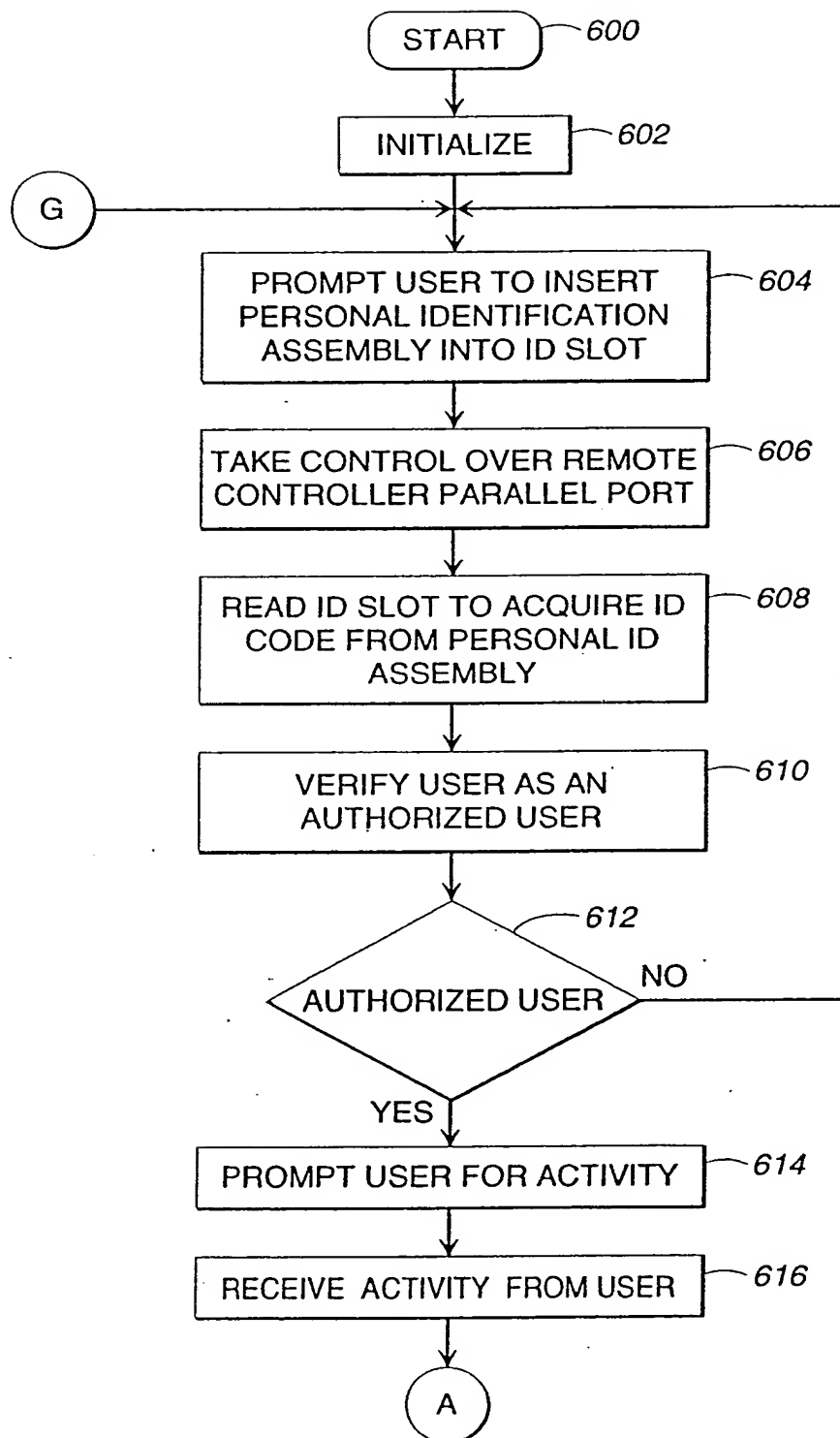
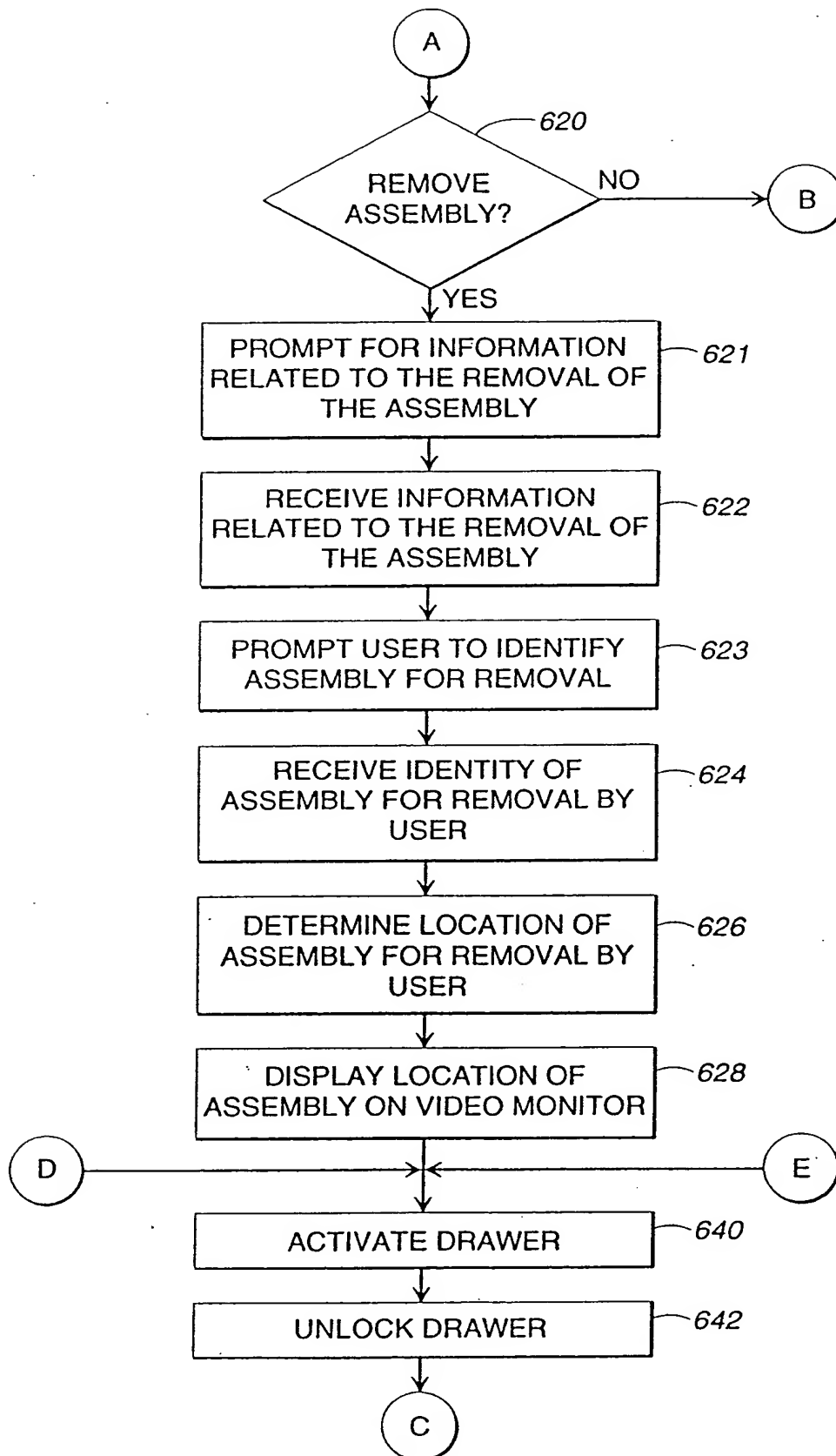


FIG. 33

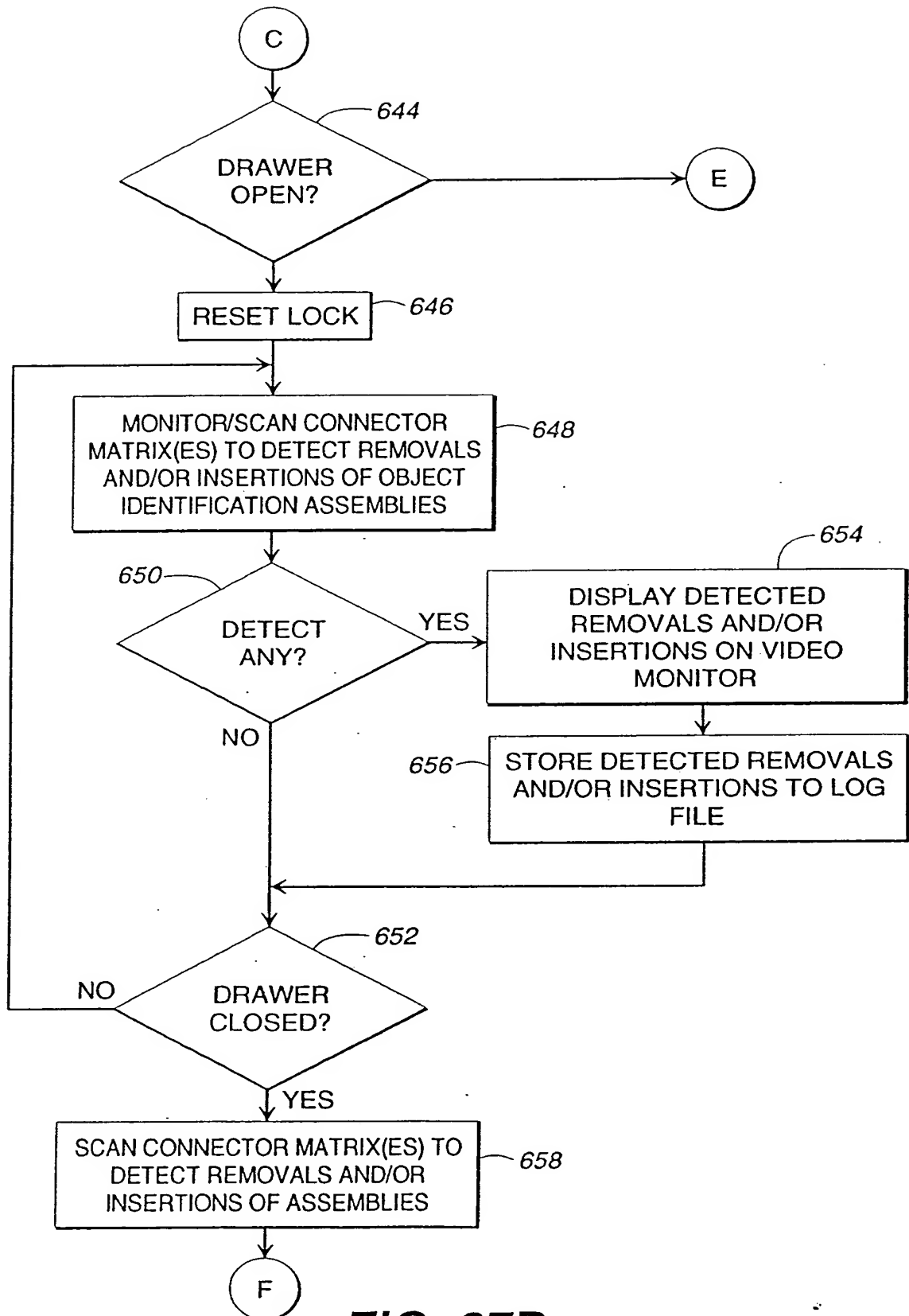




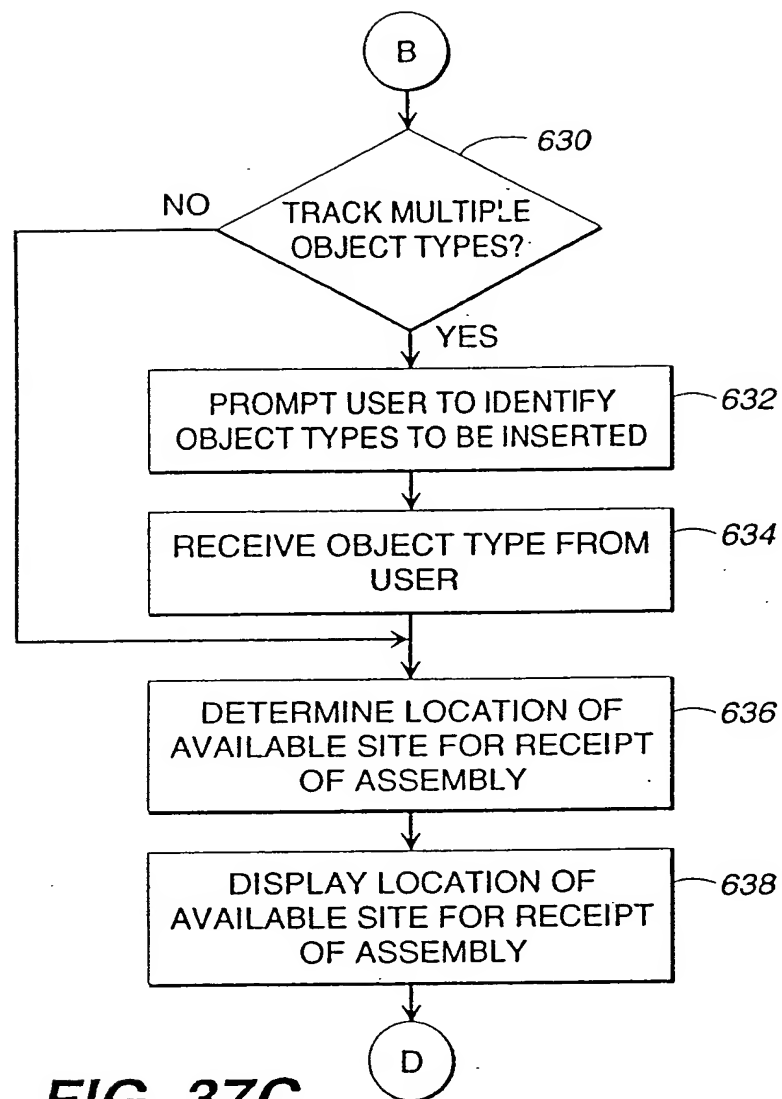
**FIG. 37A**



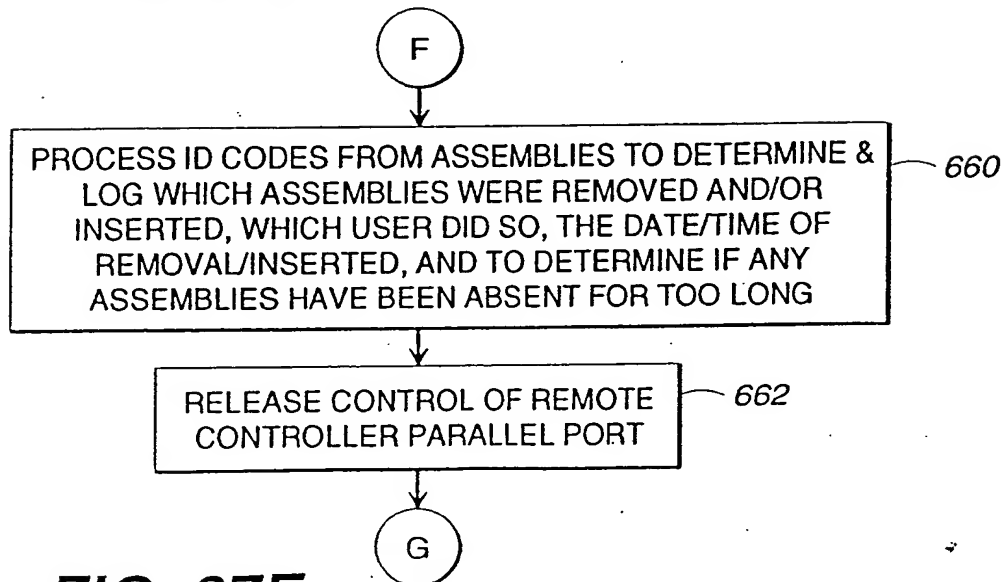
**FIG. 37B**



**FIG. 37D**



**FIG. 37C**



**FIG. 37E**